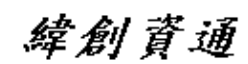
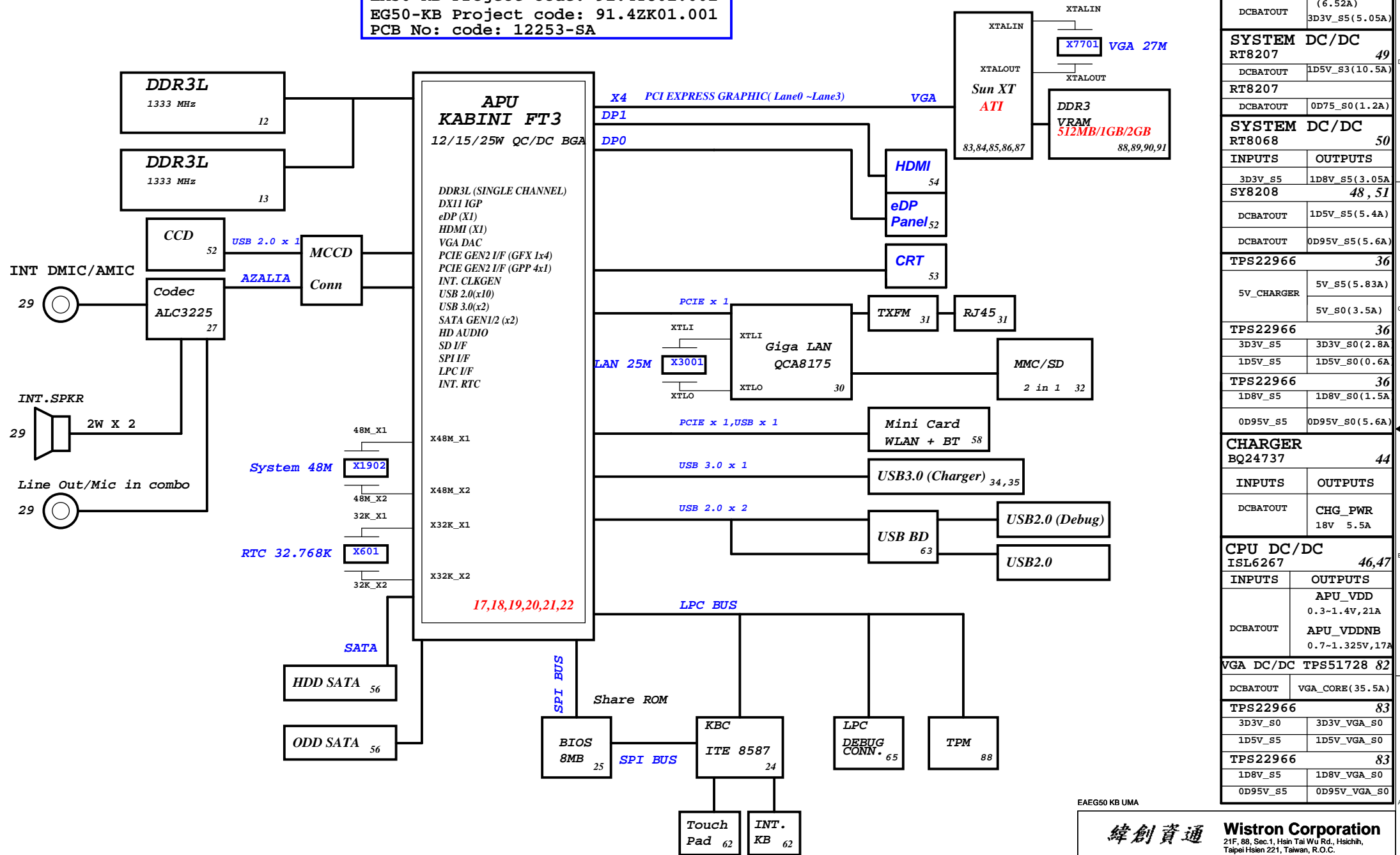


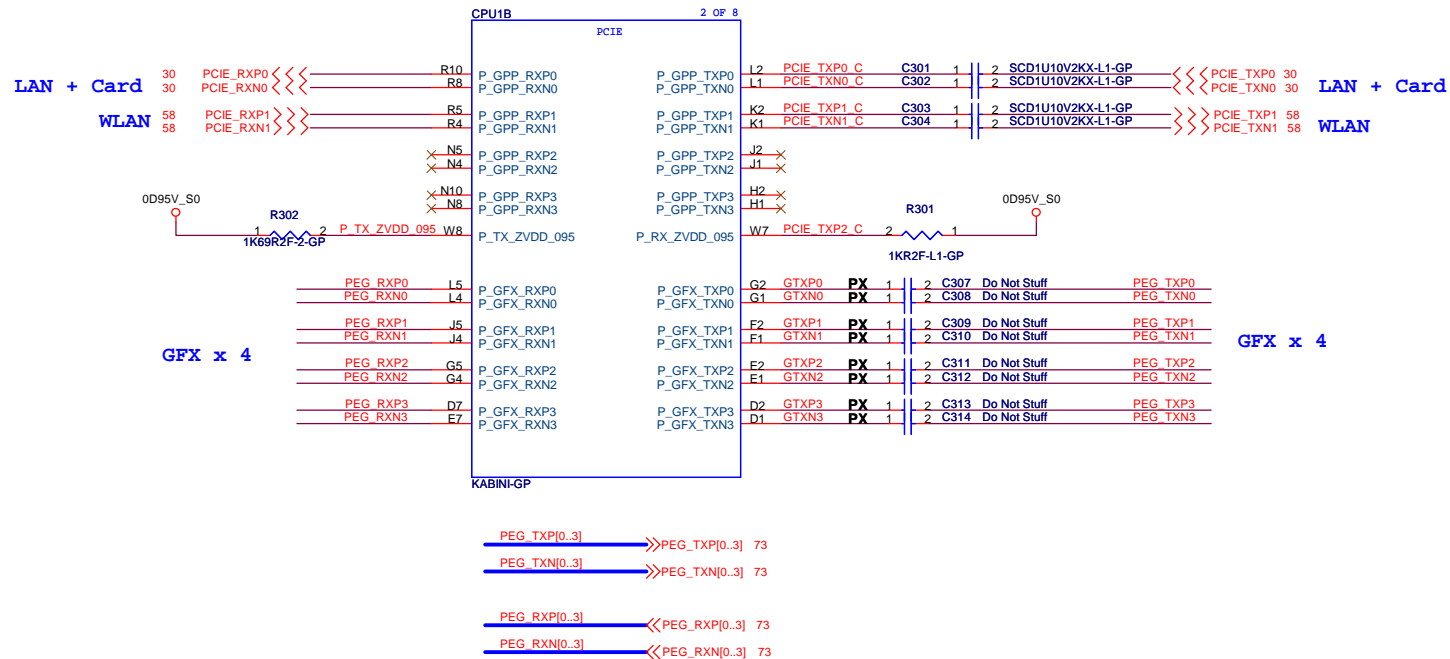
AMD KABINI EA/EG-40/50 PX /UMA Schematics Document AMD FT3 APU AMD GPU SUN XT M2/64bit

EAEG50 KB UMA

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Cover Page	
Size A4	Document Number KABINI
Date: Wednesday, October 24, 2012	Rev
Sheet 1 of 102	

EA40-KB	Project code: 91.4ZF01.001
PCB No: code: 12247-SA	
EA50-KB	Project code: 91.4YU01.001
EG50-KB	Project code: 91.4ZK01.001
PCB No: code: 12253-SA	



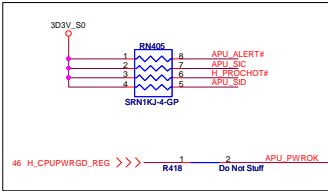


EAEG50 KB UMA

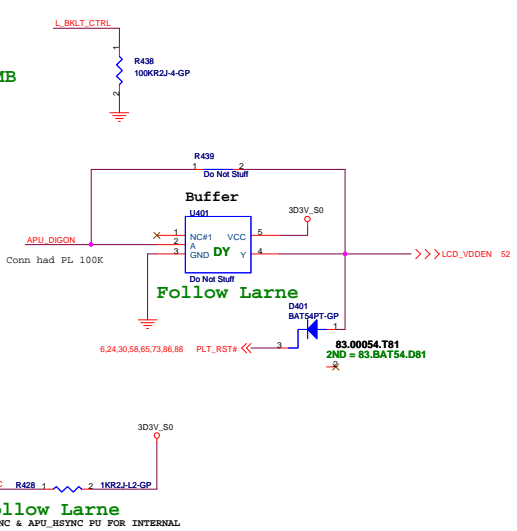
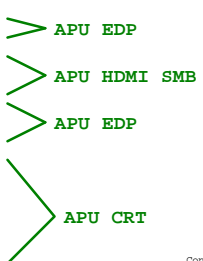
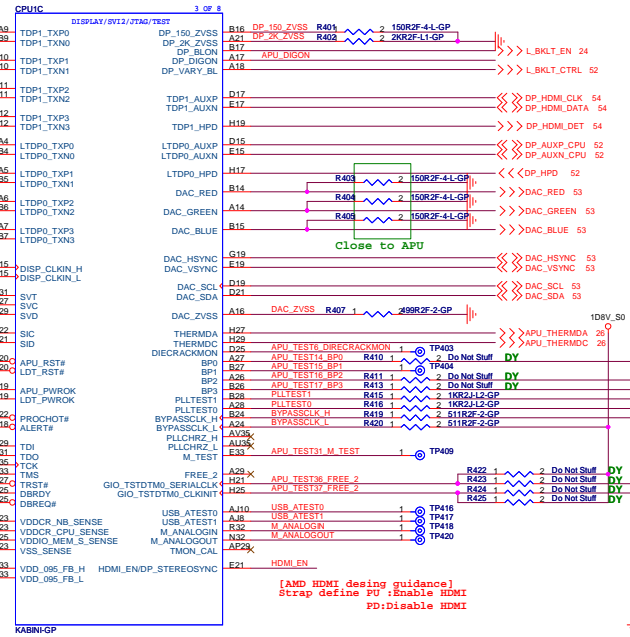
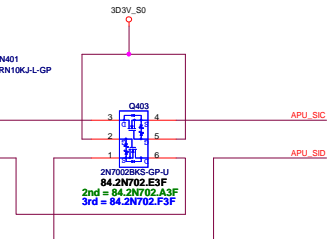
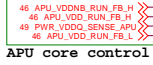
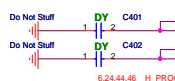
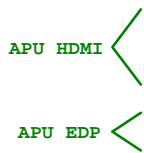
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
CPU PCIE	
Size A3	Document Number
	KABINI
Date: Monday, February 04, 2013	Rev
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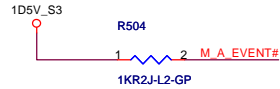
TABLE 6. PRE-PWROK METAL VID CODES

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

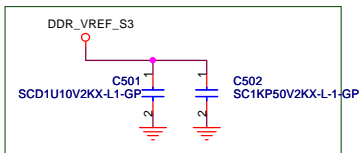


20120820 Follow Larne

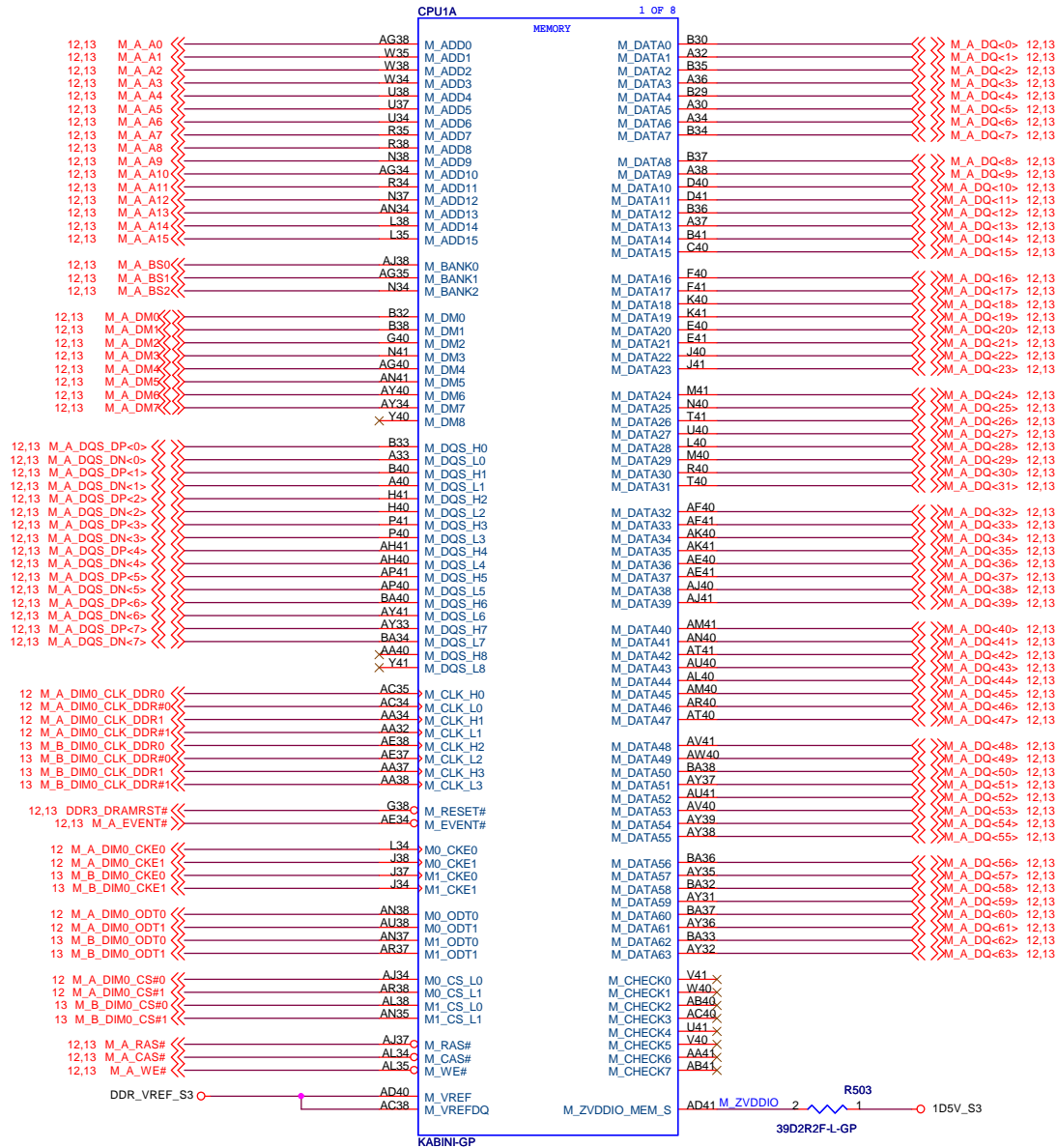


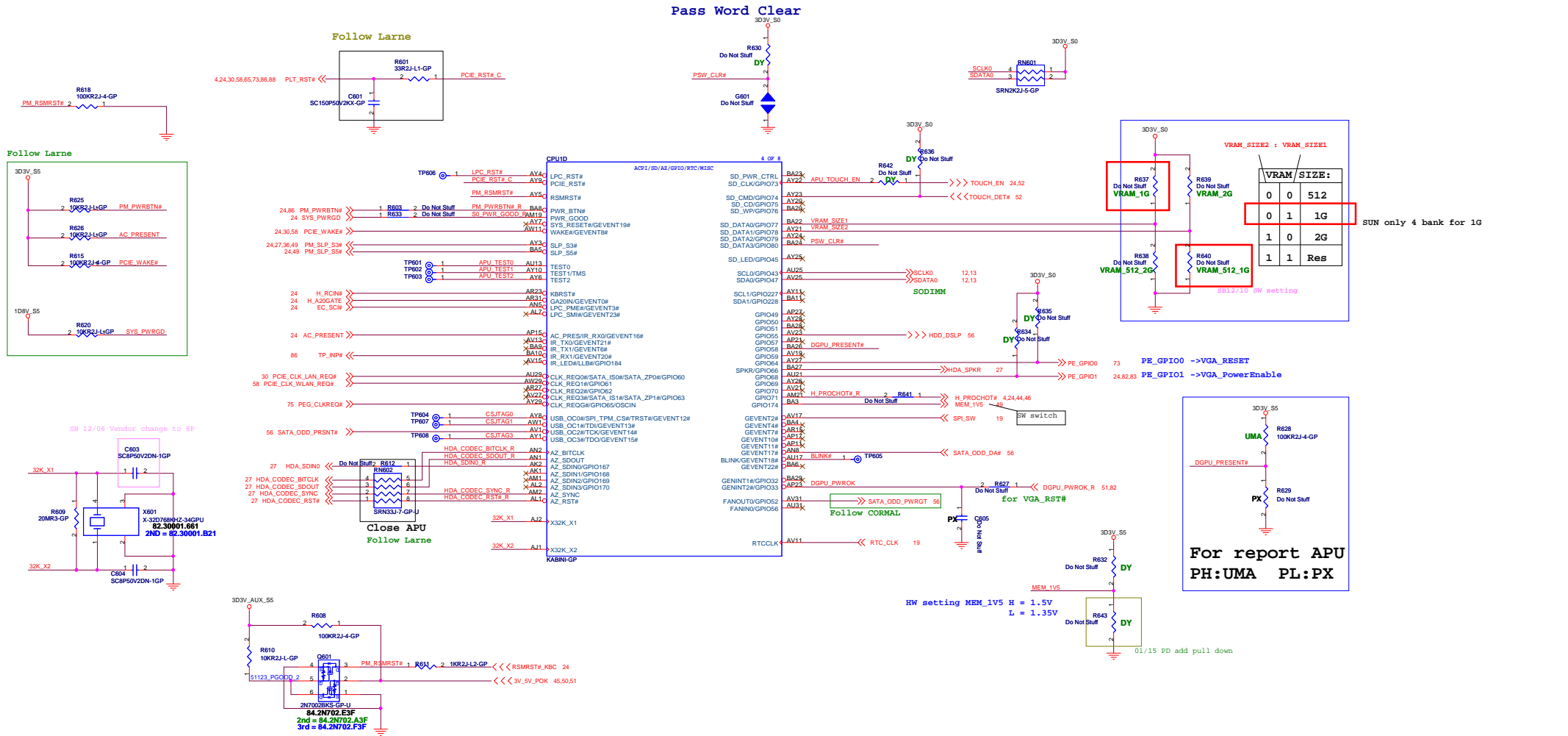


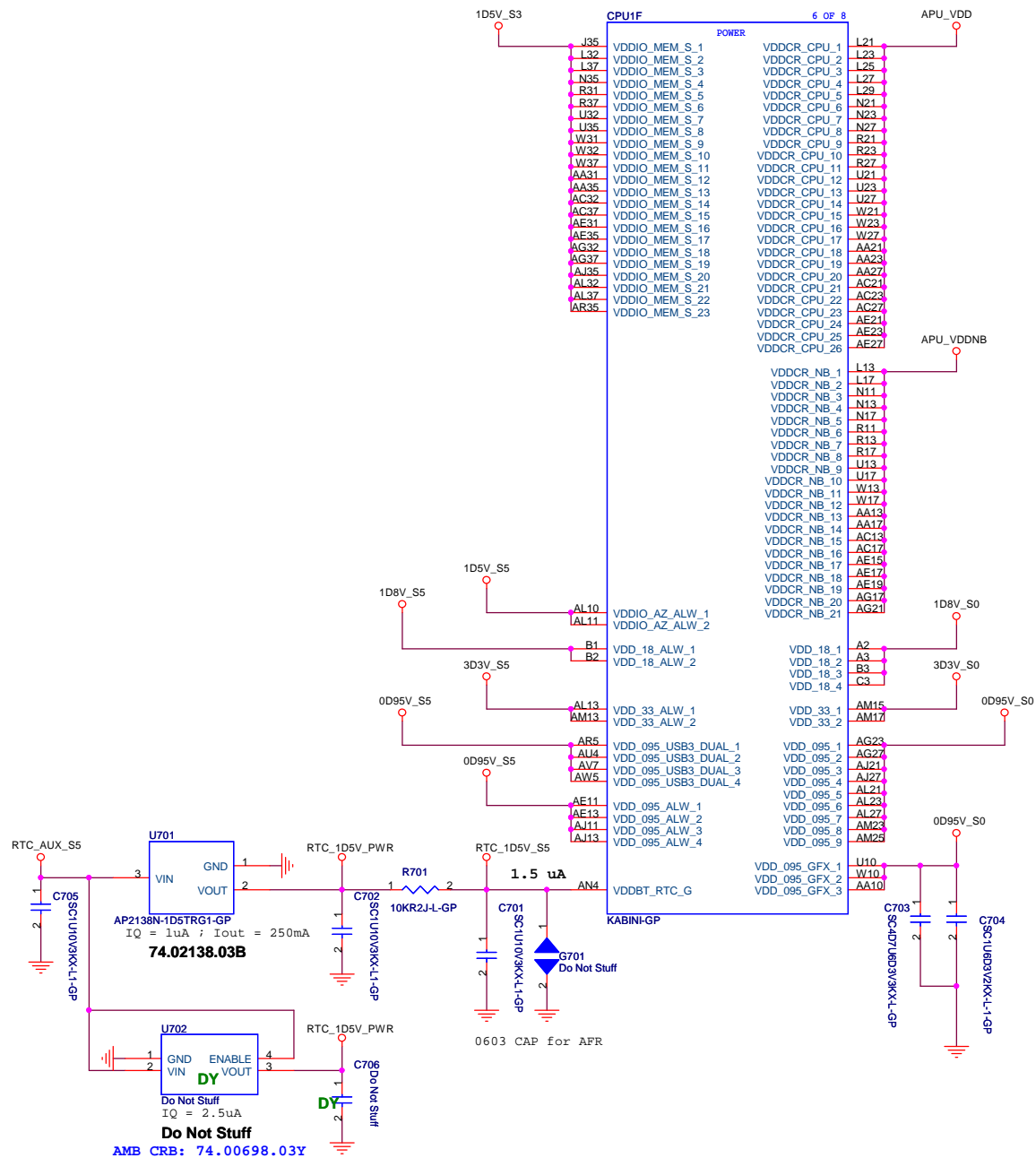
APU_VREF_DQ



LAYOUT: place them close to APU





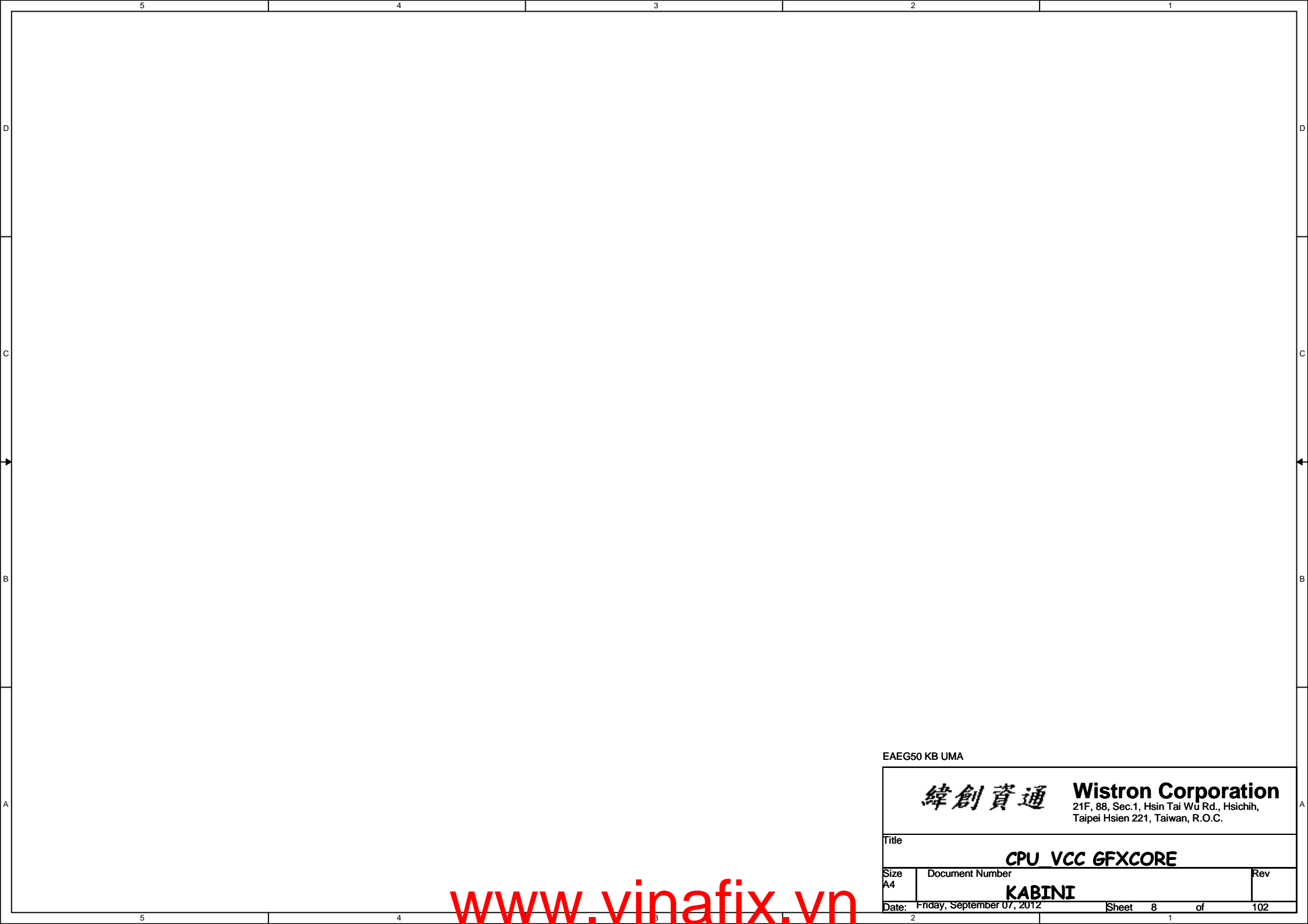


EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

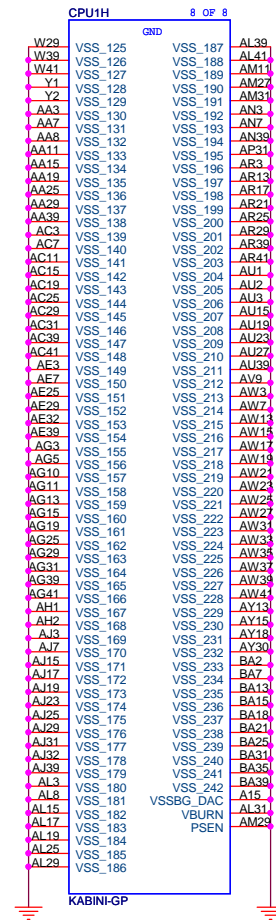
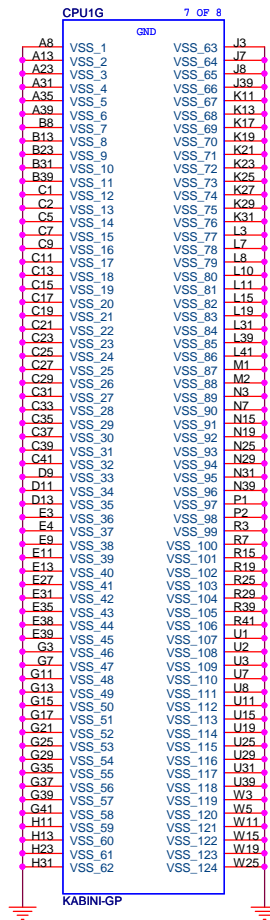
Title			CPU VCC CORE
Size	Document Number	Rev	
A3	KABINI		
Date:	Tuesday, January 15, 2013	Sheet	7 of 102

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EAEG50 KB UMA

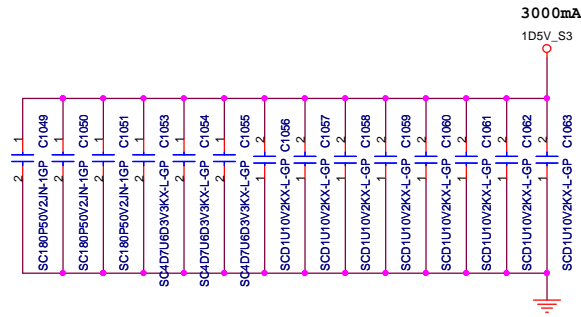
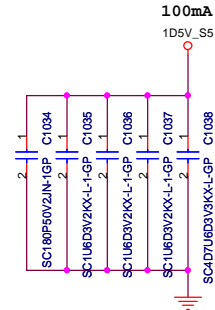
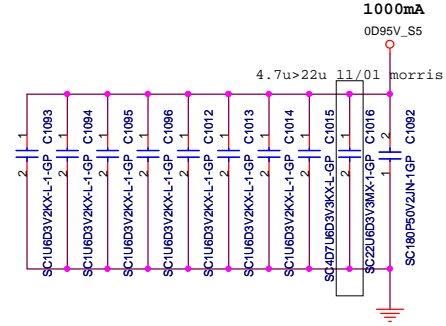
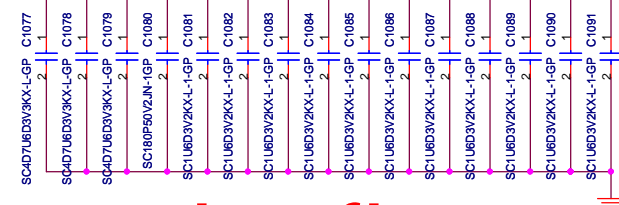
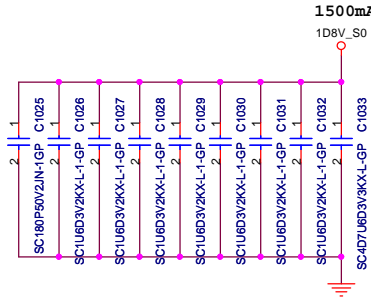
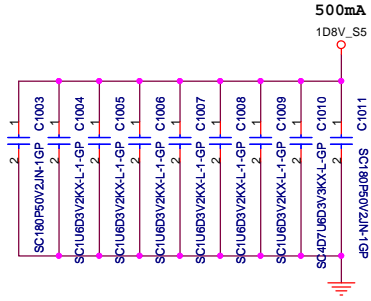
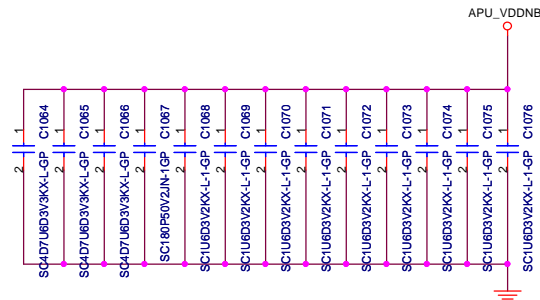
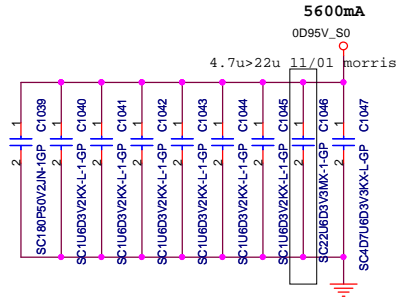
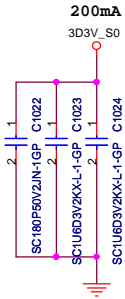
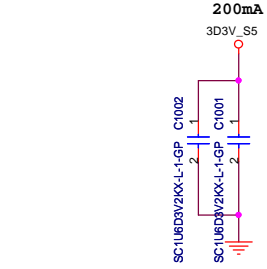
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
CPU VCC GFXCORE		
Size	Document Number	Rev
A4	KABINI	
Date:	Friday, September 07, 2012	Sheet 8 of 102



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緯創資通 Wistron Corporation
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Title			CPU VSS
Size	Document Number	Rev	
A3	KABINI		
Date:	Wednesday, November 28, 2012	Sheet	9 of 102



EAEG50 KB UMA

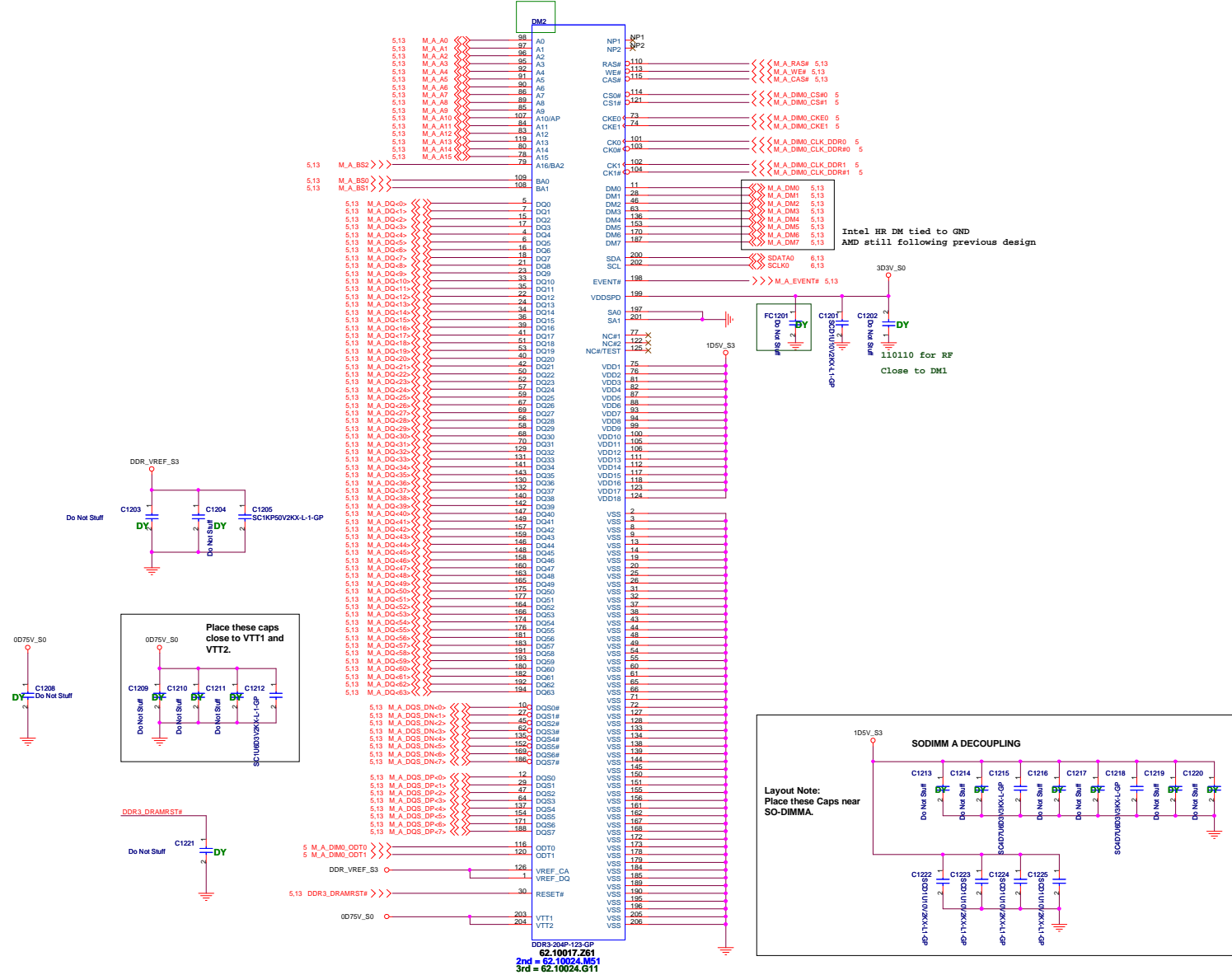
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
CPU POWER CAP1		
Size	Document Number	Rev
A3	KABINI	
Date:	Tuesday, January 15, 2013	Sheet 10 of 102

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

EAEG50 KB UMA

<div> <div>緯創資通</div> <div> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. </div> </div>		
<div> <div>Title</div> <div>CPU_POWER CAP2</div> </div>		
<div> <div>Size</div> <div>A</div> </div>	<div> <div>Document Number</div> <div>KABINI</div> </div>	<div> <div>Rev</div> <div></div> </div>
<div> <div>Date: Friday, September 07, 2012</div> <div>Sheet 11 of 102</div> </div>		

01/14 PD change location name for factory issue

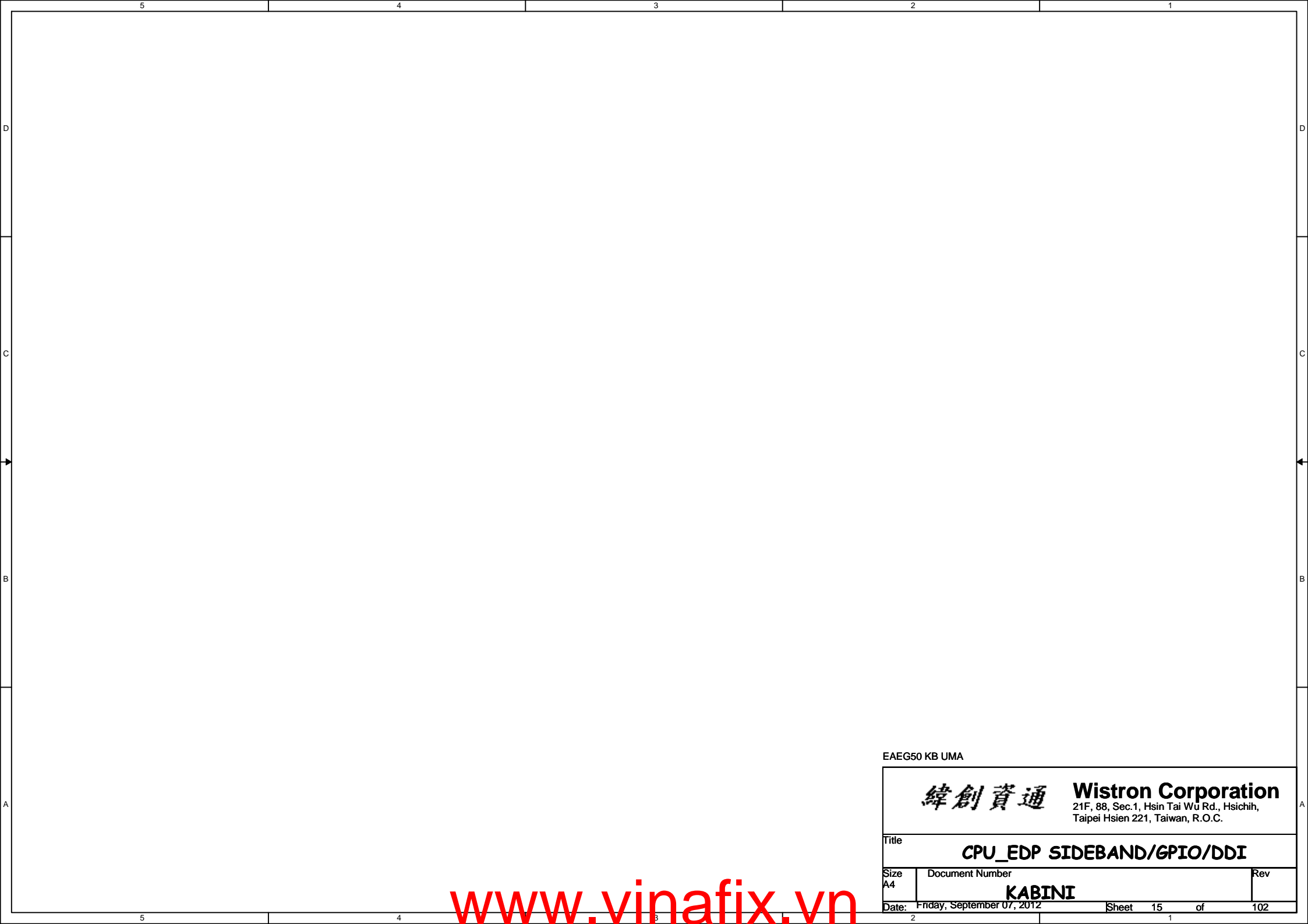


Follow JE50-SB
H = 4mm
01/15 PD remove 62.10017.X31 for factory issue



EAEG50 KB UMA

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>DDR3 SODIMM 3</div>		
Size <div>A4</div>	Document Number <div>KABINI</div>	Rev
Date: Friday, September 07, 2012		Sheet 14 of 102



EAEG50 KB UMA

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>CPU_EDP SIDEBAND/GPIO/DDI</div>		
Size <div>A4</div>	Document Number <div>KABINI</div>	Rev
Date: Friday, September 07, 2012		Sheet 15 of 102



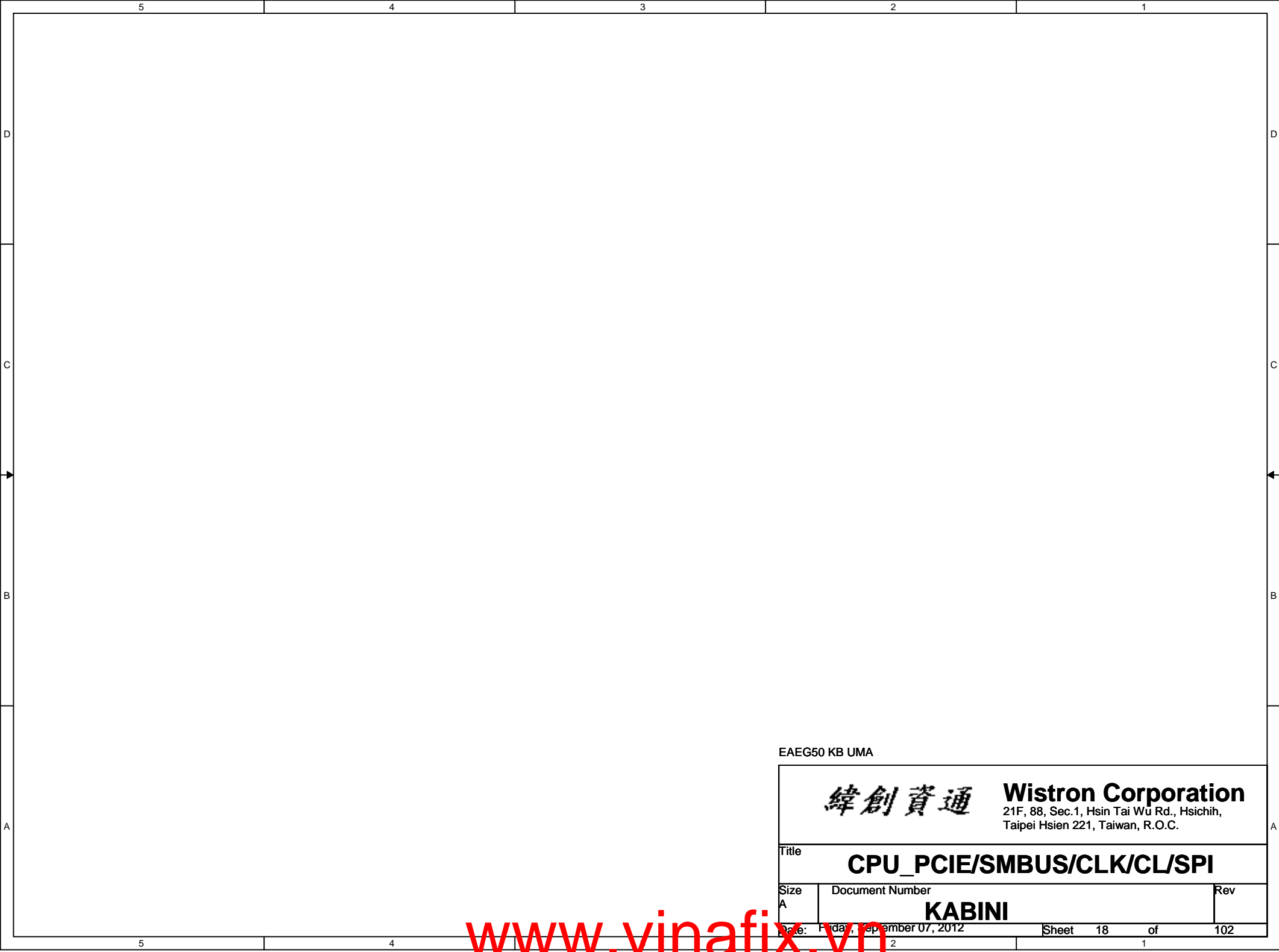
EAEG50 KB UMA

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
CPU PCIE/USB		
Size	Document Number	Rev
A4	KABINI	
Date: Friday, September 07, 2012		Sheet 16 of 102

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

EAEG50 KB UMA

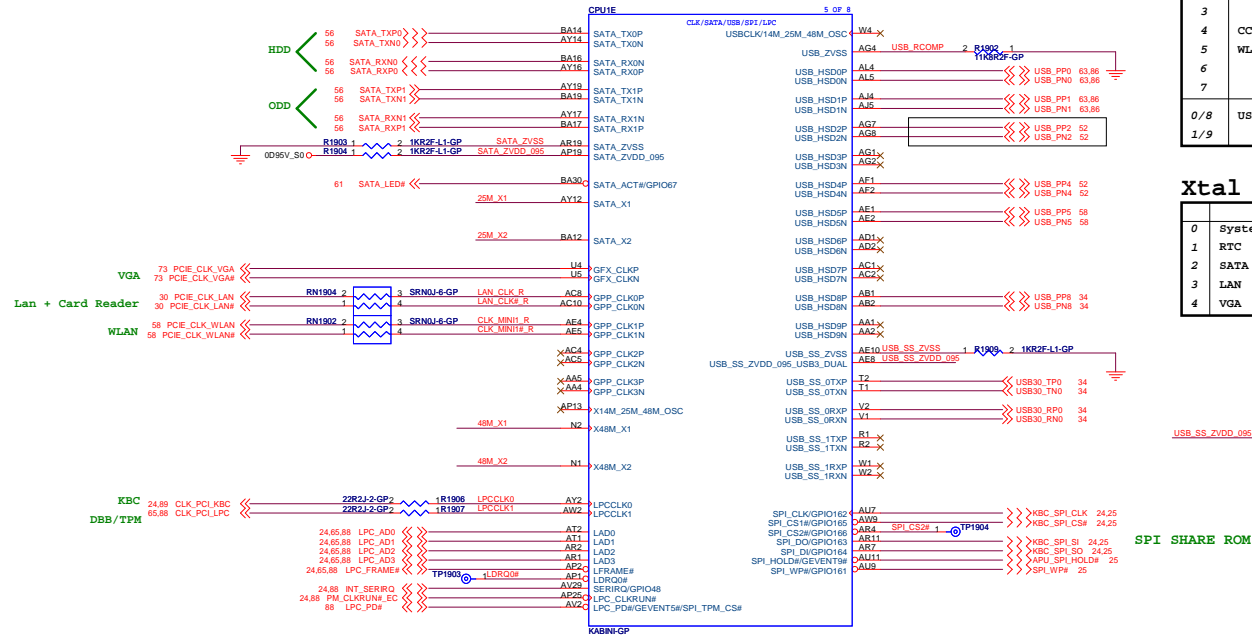
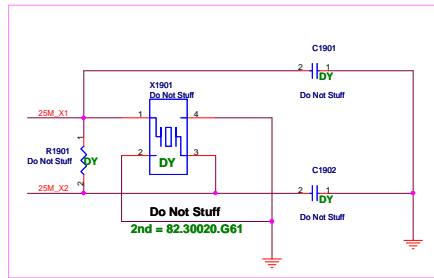
<div> <div>緯創資通</div> <div> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. </div> </div>	
<div> <div>Title</div> <div>CPU DMI/FDI/PM</div> </div>	
<div> <div>Size</div> <div>A</div> </div>	<div> <div>Document Number</div> <div>KABINI</div> </div>
<div> <div>Rev</div> <div></div> </div>	
<div> <div>Date: Friday, September 07, 2012</div> <div>Sheet 17 of 102</div> </div>	



EAEG50 KB UMA

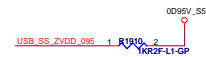
<div><div>緯創資通</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title CPU_PCIE/SMBUS/CLK/CL/SPI		
Size A	Document Number KABINI	Rev
Date: Friday, September 07, 2012		Sheet 18 of 102

0	HDD
1	ODD



Pair	Device
0	USB2.0 Debug (DB Conn)
1	USB2.0 (DB Conn)
2	Touch Panel
3	
4	CCD (CCD Conn)
5	WLAN + BT (Mini PCI-E)
6	
7	
0/8	
1/9	USB3.0 & USB 2.0 Charger (MB)

		CLK
0	System & USB	48M
1	RTC	32.768K
2	SATA	25M
3	LAN	25M
4	VGA	27M



	LPC_CLK0	LPC_CLK1	LPCFRAME 1	EXPBOARD_PCIE_PWREN#	RTC_CLK
PULL HIGH	BOOT FAIL TIMER ENABLED	CLIRGEN ENABLED (DEFAULT)	SPI ROM (DEFAULT)	1.0V SPI ROM (DEFAULT)	NORMAL POWER UP/RESET TIMING (DEFAULT)
PULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)	CLIRGEN DISABLED	LPC ROM	3.0V SPI ROM	FAST POWER UP/RESET TIMING FOR SIMULATION



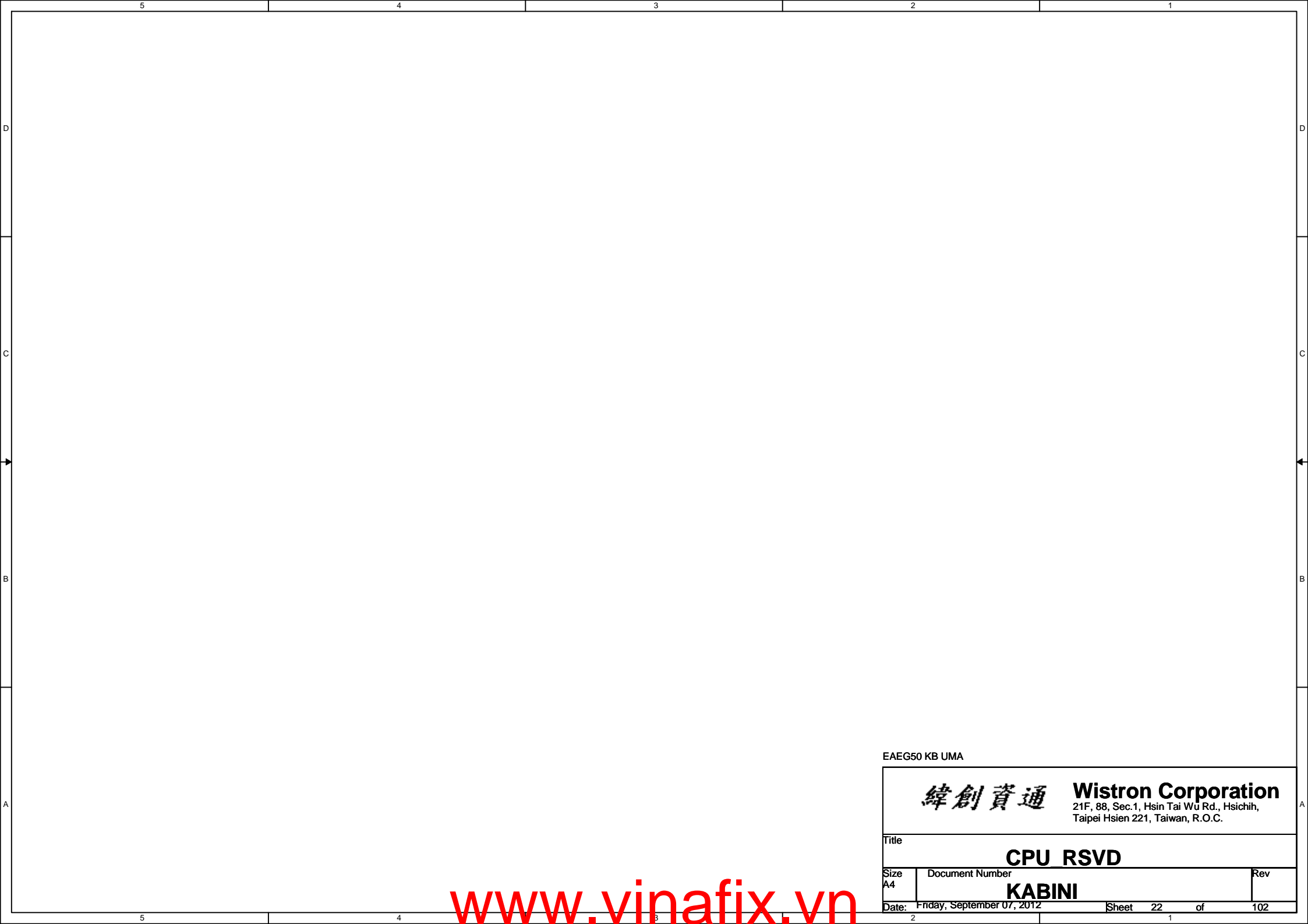
EAEG50 KB UMA

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
CPU GPIO/MISC		
Size	Document Number	Rev
A4	KABINI	
Date:	Friday, September 07, 2012	Sheet 20 of 102



EAEG50 KB UMA

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
CPU POWER1		
Size	Document Number	Rev
A4	KABINI	
Date: Friday, September 07, 2012		Sheet 21 of 102



EAEG50 KB UMA

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
CPU RSVD		
Size	Document Number	Rev
A4	KABINI	
Date: Friday, September 07, 2012		Sheet 22 of 102



EAEG50 KB UMA

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
CPU VSS		
Size	Document Number	Rev
A4	KABINI	
Date: Friday, September 07, 2012		Sheet 23 of 102

Thermal sensor NCT 7718W

[illegible]

2. System Sensor, Put on palm rest

20120831

[SC 12/12 for change Thermal SMBus with APU](#)

NCT7718W-GP
74.07718.0B9

SC for EA50 & EA40: 74.83771.ABG

SC EA50 DY RN2604 , mount RN2603

24,86 FAN1_PWM >>>—
86 FAN_TACH1_C >>>—

For AFTE

20.F1579.004
2nd = 20.F1637.004

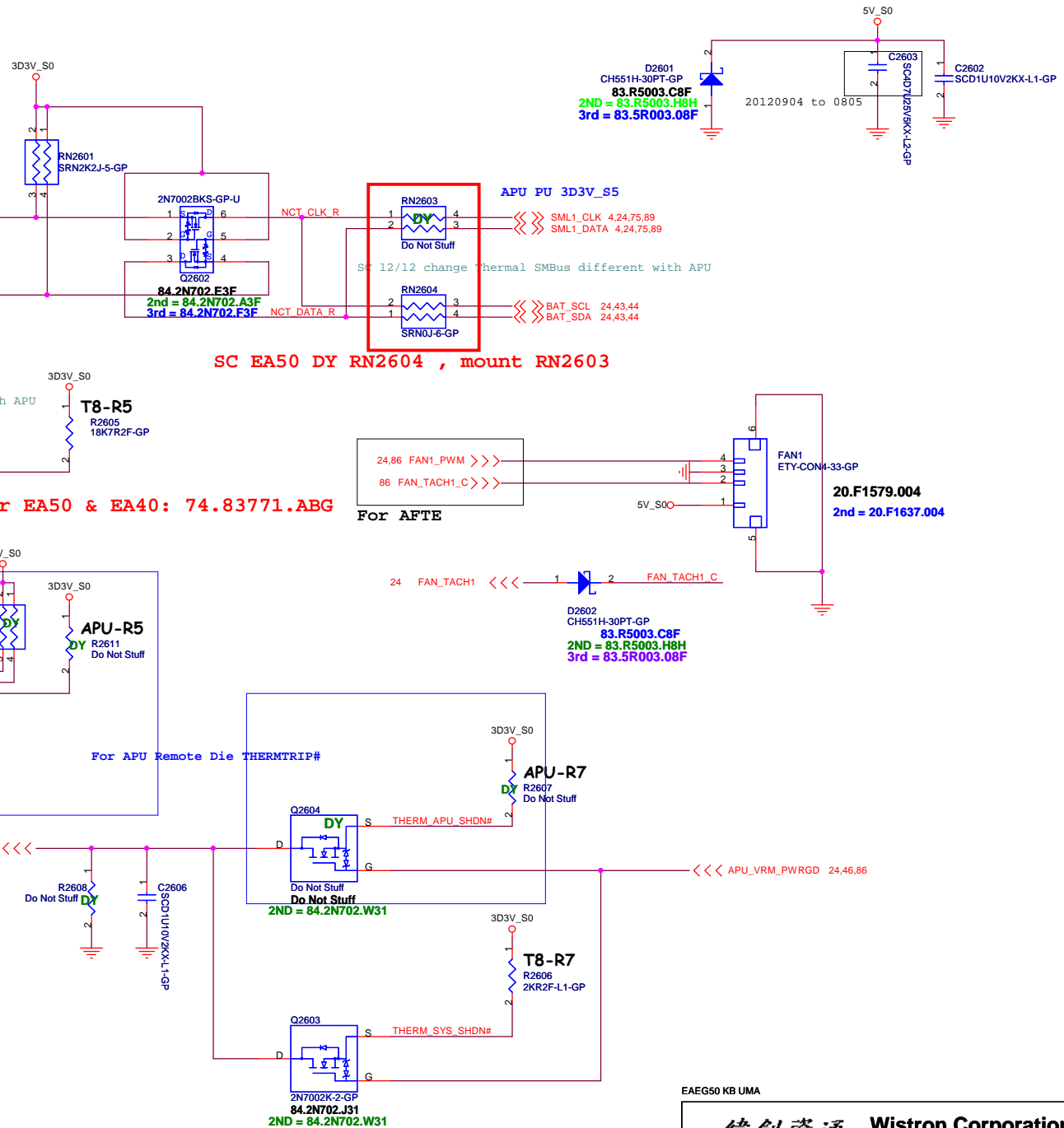
ALERT# /T CRIT#
Pull-up R̄esistor

	R7				
	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
R5					
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point

T8=85 degree
SYS=85 degree
APU=125 degree

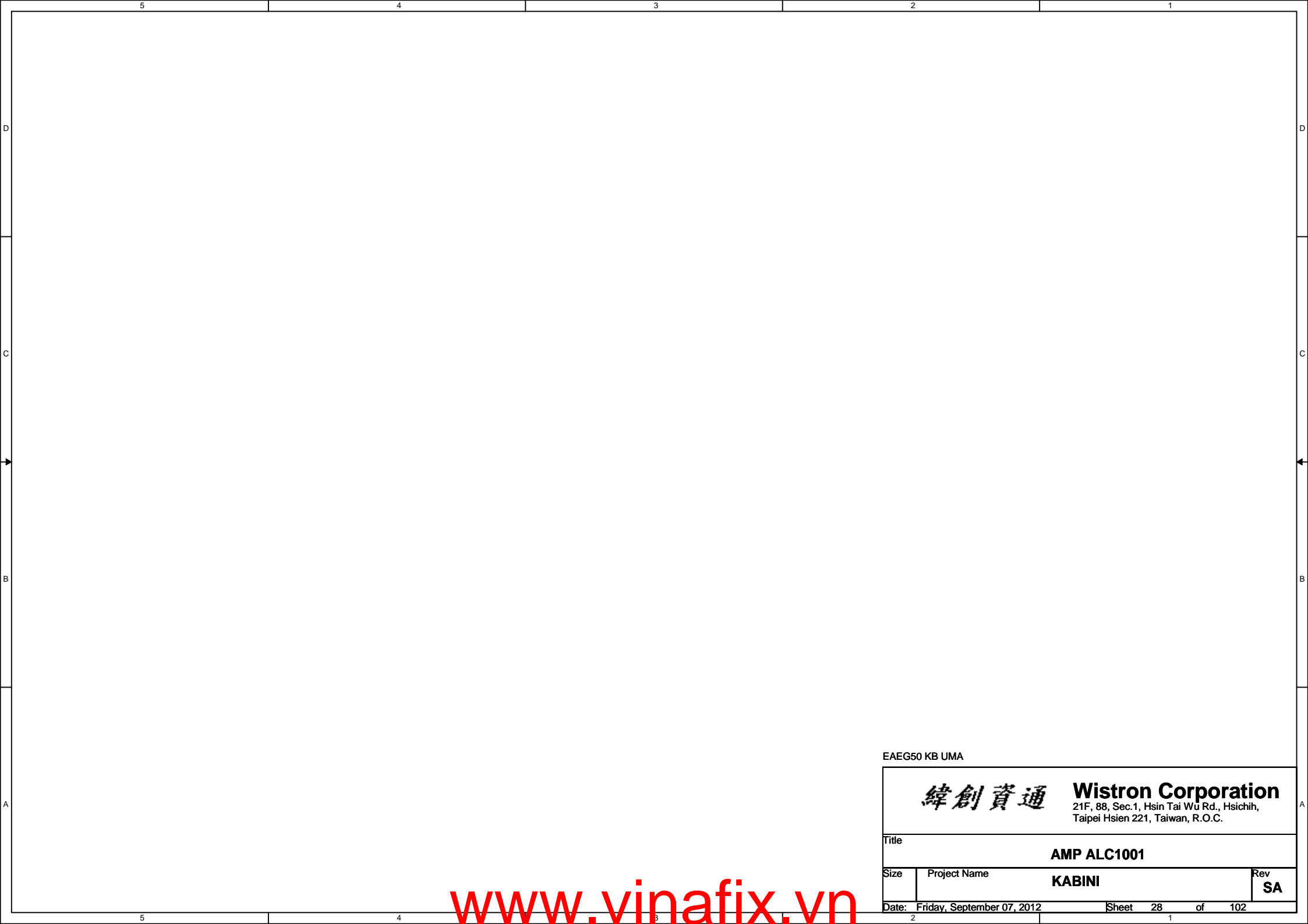
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
Thermal 7718/Fan Controller P2793			
Size	Project Name		Rev
	KABINI		SA
Date:	Monday, February 04, 2013		Sheet 26 of 102



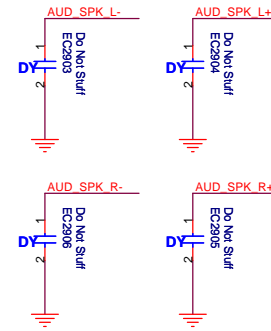
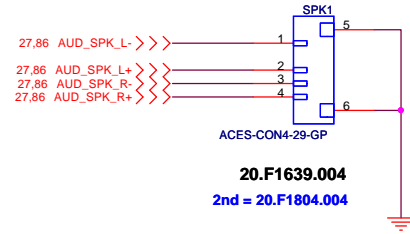
EAEG50 KB UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AMP ALC1001			
Size	Project Name		Rev
	KABINI		SA
Date: Friday, September 07, 2012		Sheet 28 of 102	

SSID = AUDIO

Speaker

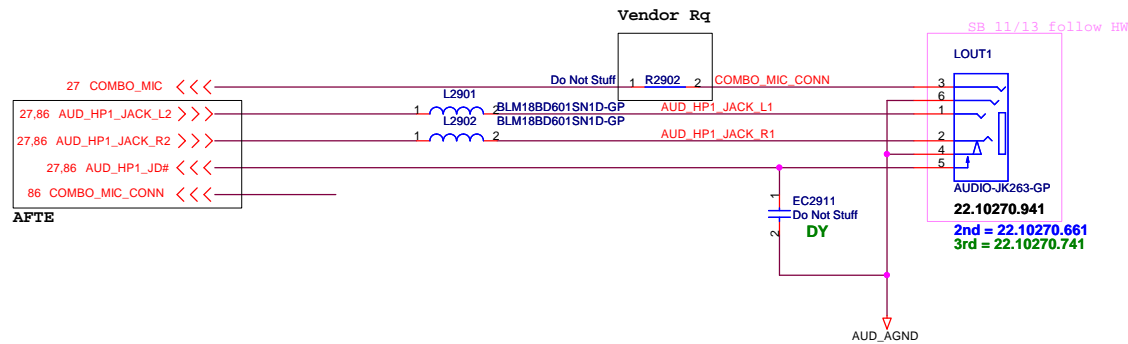
2W 4ohm X 2 speaker



Layout Note:

Trace width=40mil

Combo Jack



EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Audio Jack	
Size	Project Name		KABINI	Rev SA
Date:	Monday, February 04, 2013		Sheet 29	of 102

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Power-On-Strapping Table

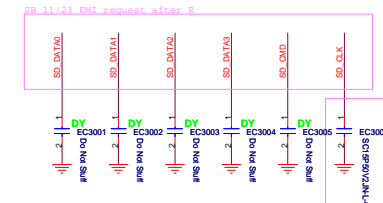
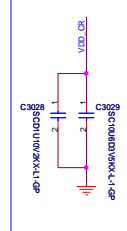
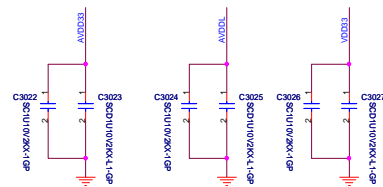
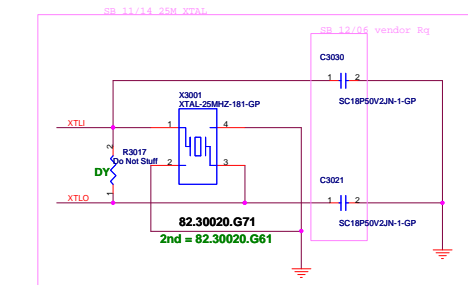
Pin	Description
LED[1]	1 Switch mode regulator (SWR) select 0 Linear regulator (LDO) select
LED[3]	1 25MHz clock input 0 48MHz clock input
[CRIO14, CRIO7]	10 1. Support xD, not support SPI. 2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFuse. 01 1. Support SPI, not support xD. 2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFuse. 11 1. Not support xD, not support SPI. 2. Only Support PPS, PPS always at CRIO13.

PPS is used for IEEE 1588 timing synchronization and is an output pin to output an accurate 1Hz clock. Currently this pin can be floating.

Check!!

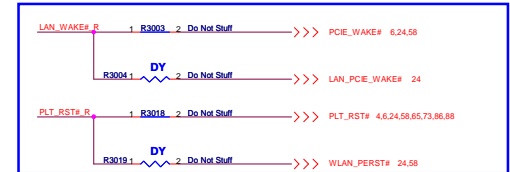
ISOLATn is active low to isolate the whole chip to place in lowest power consumption mode.

place at chip side FAE suggest



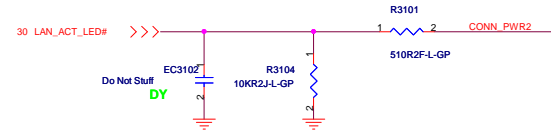
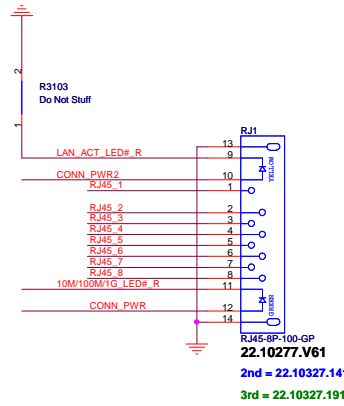
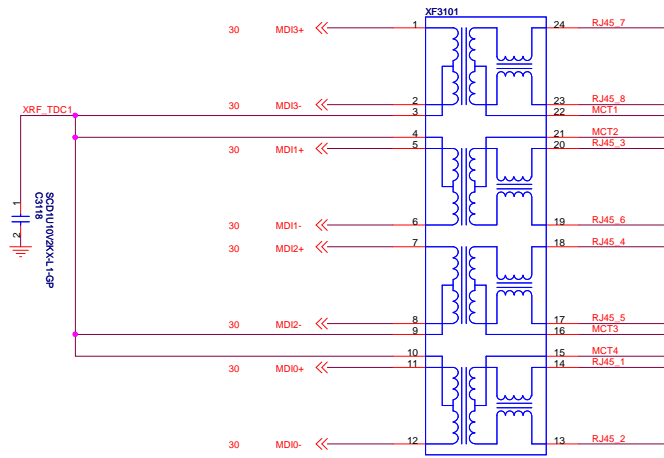
SB 12/04 vendor Bq mount

系統端已PH



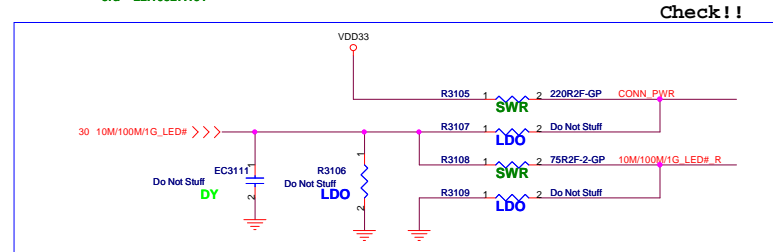
xD_CEn	xD_CEn
CRI014	xD_ALE
CRI013	xD_RDBYn
CRI012	xD_RStn
CRI011	SDMMC_Clk
CRI010	MMC DAT7
CRI009	MMC DAT6
CRI008	MMC DAT5
CRI007	MMC DAT4
CRI006	SD_WP
CRI005	SDMMC_CLK
CRI004	SDMMC_CMD
CRI003	SDMMC DAT3
CRI002	SDMMC DAT2
CRI001	SDMMC DAT1
CRI000	SDMMC DAT0

SSID = LAN

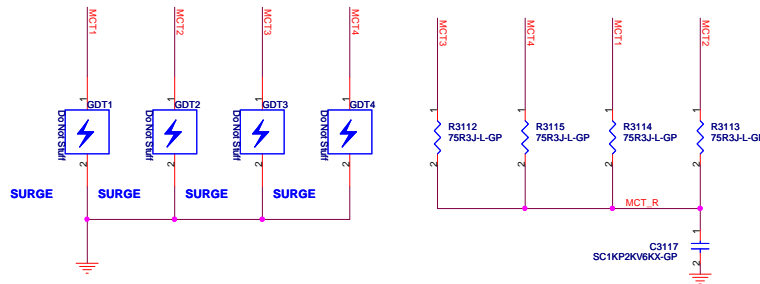
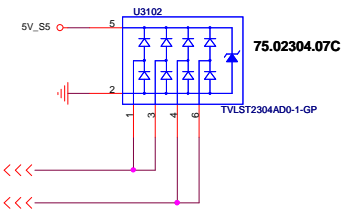
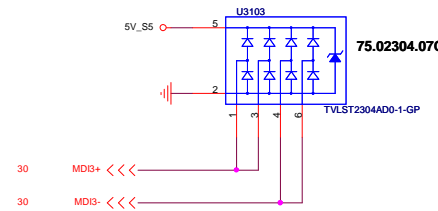
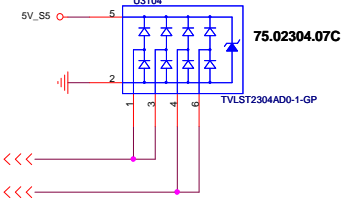
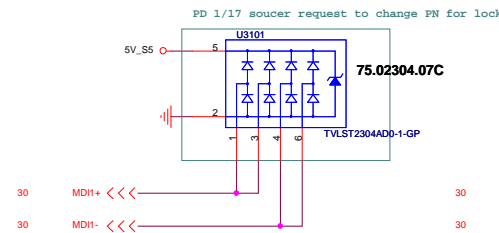
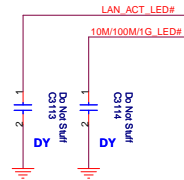
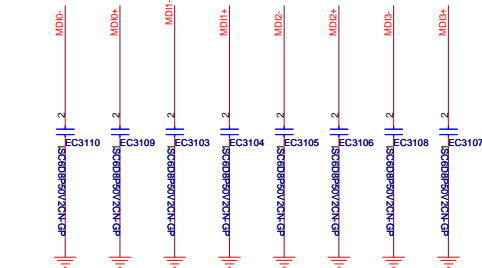
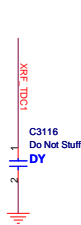


86 RJ45_1 >>>
86 RJ45_2 >>>
86 RJ45_3 >>>
86 RJ45_4 >>>
86 RJ45_5 >>>
86 RJ45_6 >>>
86 RJ45_7 >>>
86 RJ45_8 >>>
86 LAN_ACT_LED#_R >>>
86 10M/100M/1G_LED#_R >>>
86 CONN_PWR >>>
86 CONN_PWR2 >>>

For AFTE



Check !!



EAEG50 KB UMA

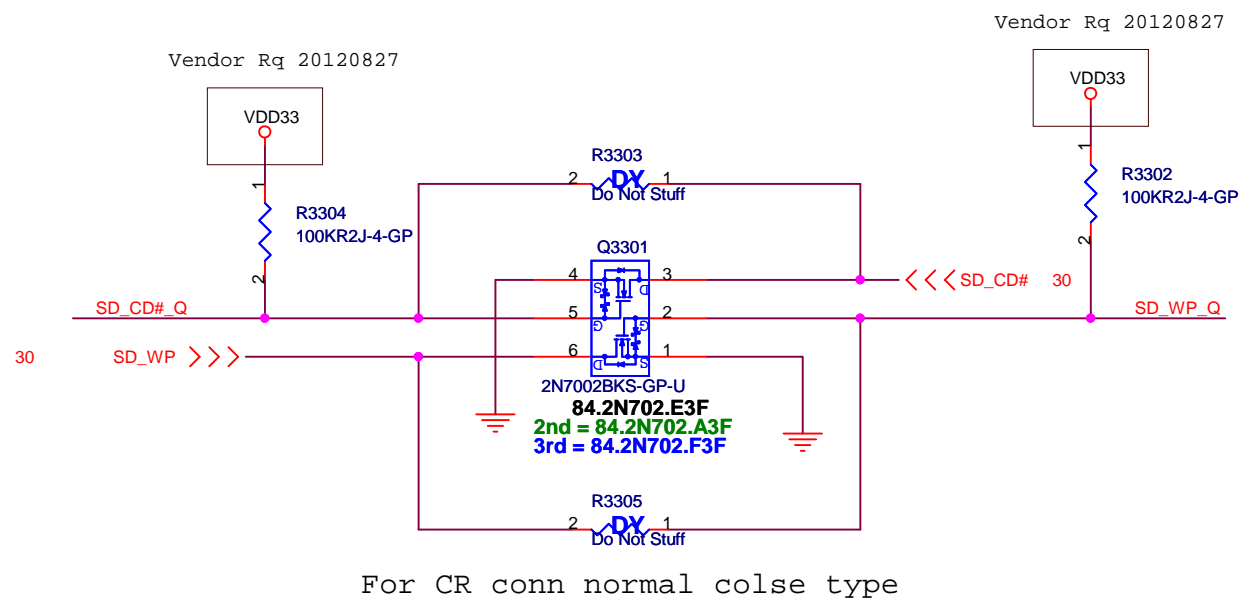
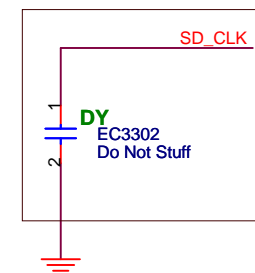
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title LAN CONNECTOR	
Size KABINI	
Date: Monday, February 04, 2013	Sheet 31 of 102



EAEG50 KB UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Card Reader IC			
Size	Project Name		Rev
	KABINI		SA
Date: Friday, September 07, 2012		Sheet 32 of 102	

SD//MS Card Reader



緯創資通

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

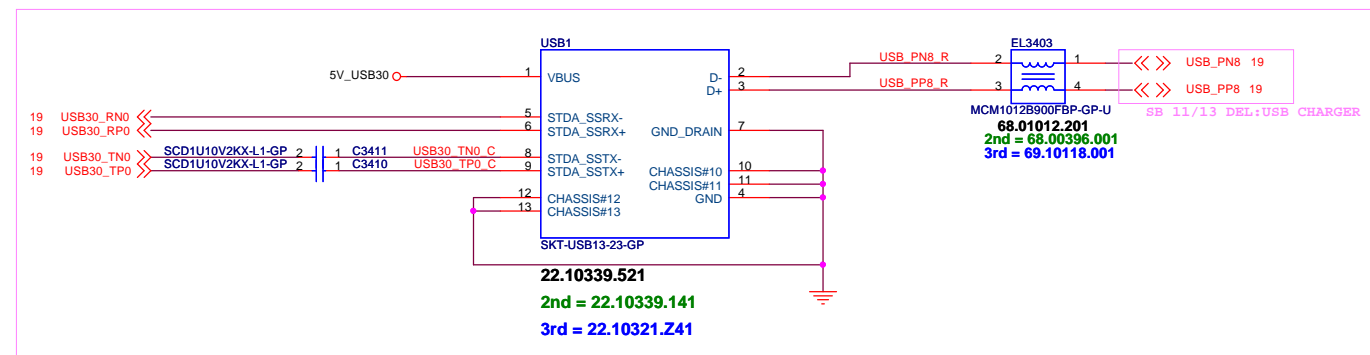
CARD Reader CONN

KABINI

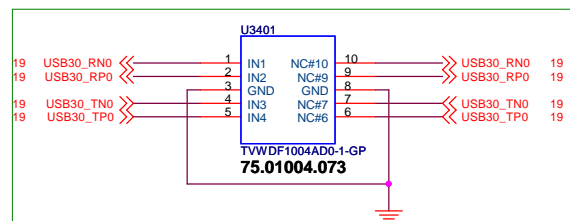
Rev
SA

Sheet 33 of 102

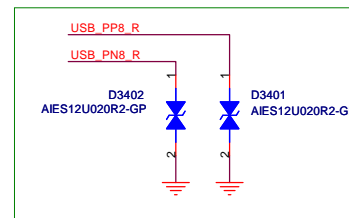
USB 2.0 CONTACT PIN		USB 3.0 CONTACT PIN	
PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
1	VBUS	5	StdA_SSRX-
2	D-	6	StdA_SSRX+
3	D+	7	GND_DRAIN
4	GND	8	StdA_SSTX-
		9	StdA_SSTX+



SB 11/13 Change USB30 P/N



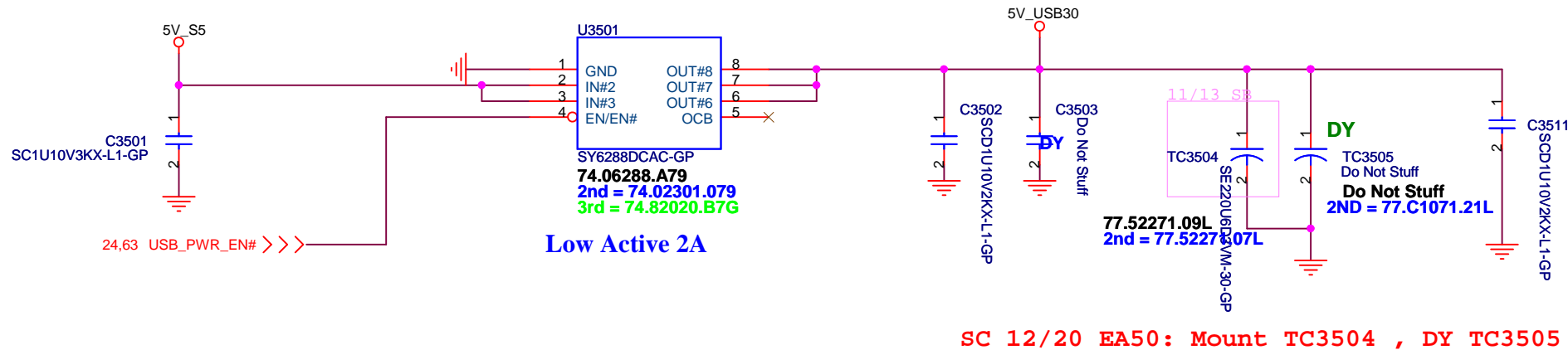
2/4 PD for Factory USB ESD issue.



1/28 PD for Factory USB ESD issue.

EAEG50 KB UMA

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
USB 3.0 Port			
Size	Project Name	Rev	
	KABINI	SA	
Date:	Monday, February 04, 2013	Sheet	34 of 102



EAEG50 KB UMA

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB_Charger

Size

Project Name

KABINI

Rev

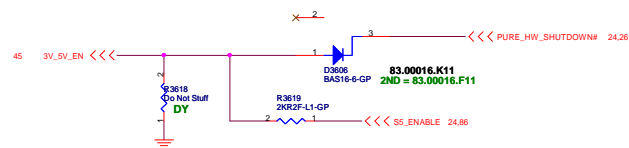
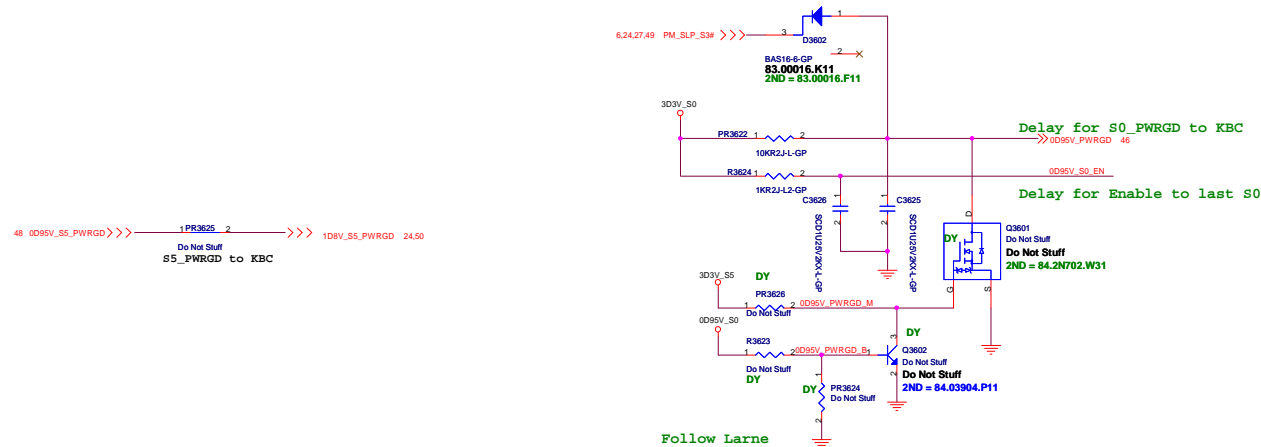
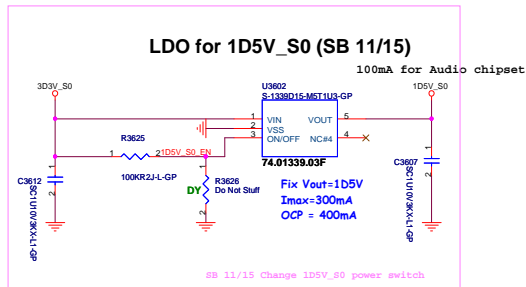
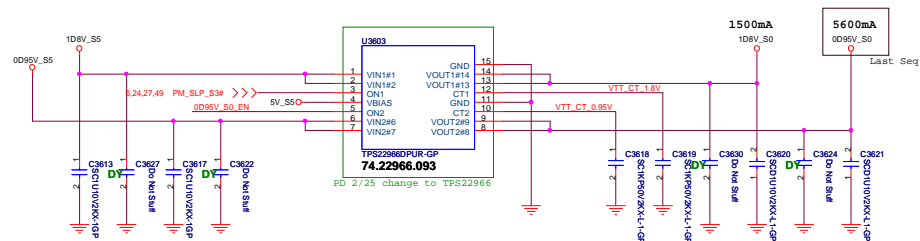
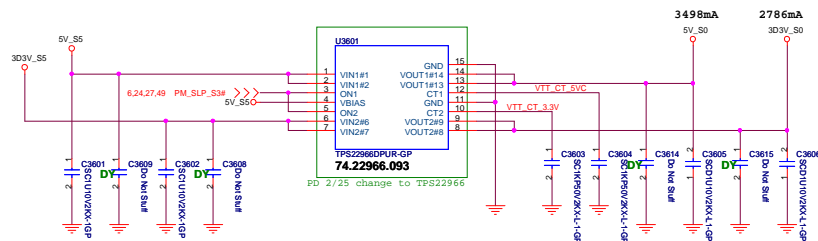
SA

Date: Monday, February 04, 2013

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Power Sequence

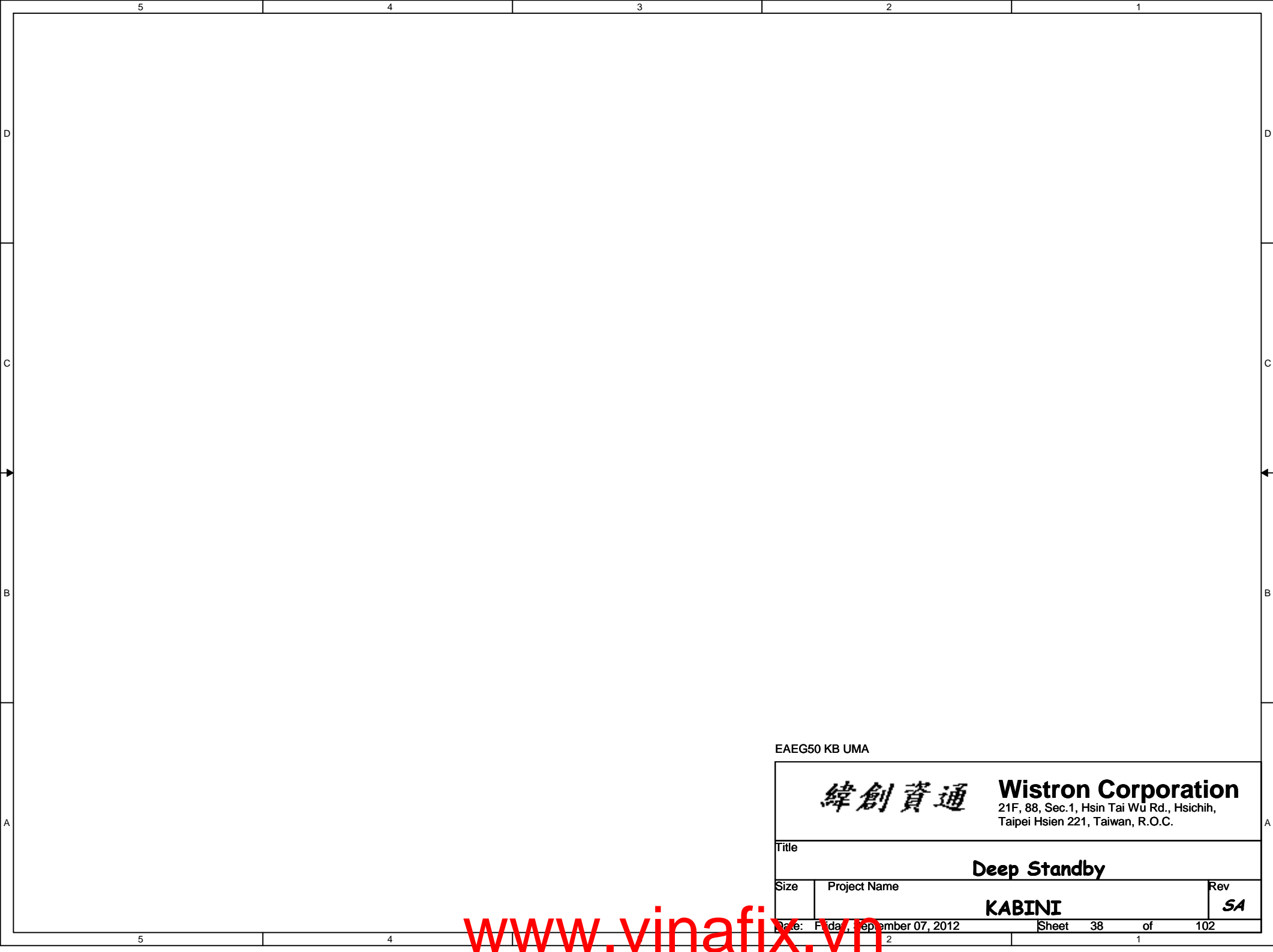


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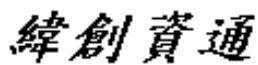


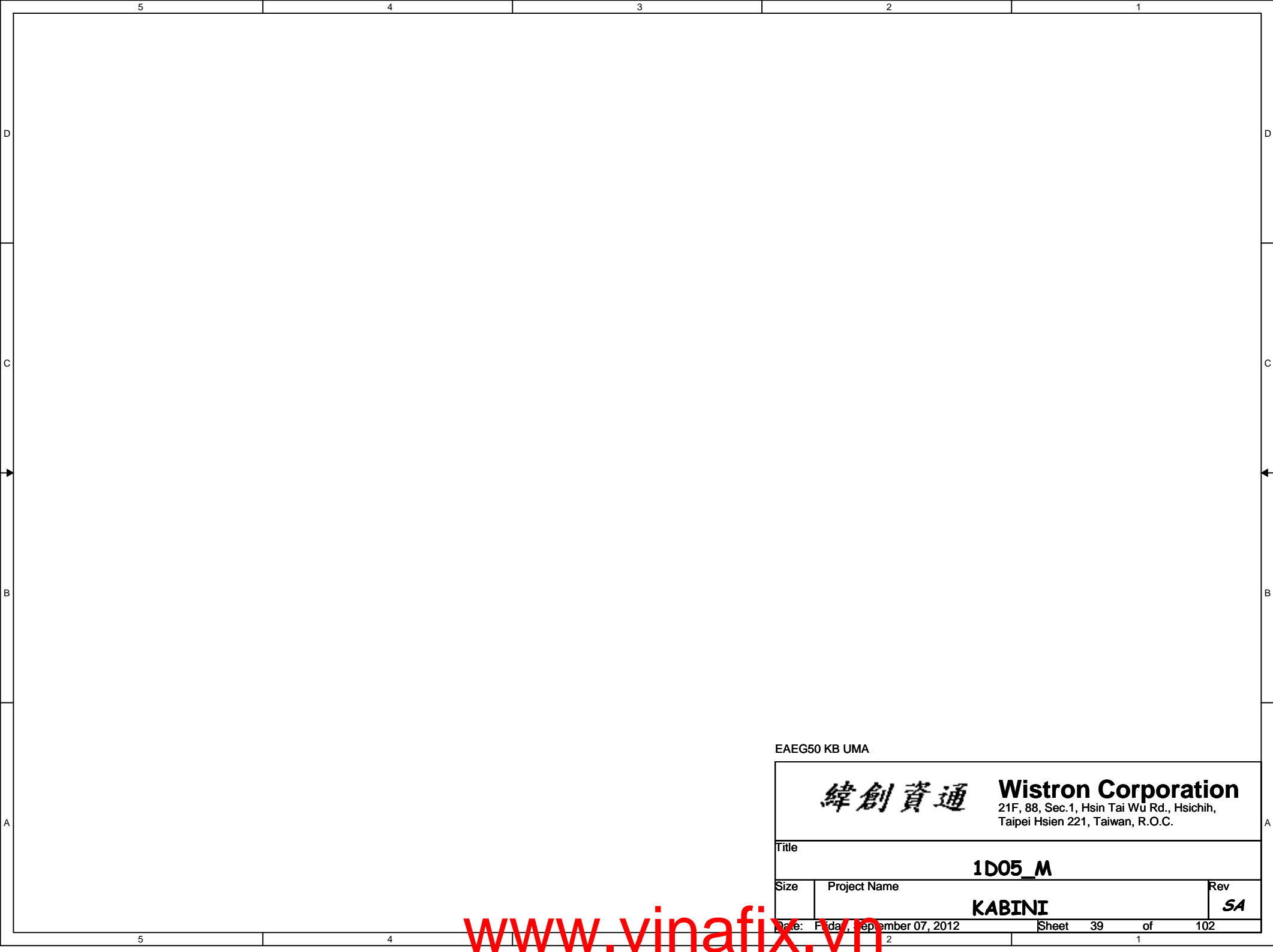
EAEG50 KB UMA

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title ADAPTER OCP / S3 reduction		
Size	Project Name KABINI	Rev SA
Date: Thursday, January 24, 2013		Sheet 37 of 102



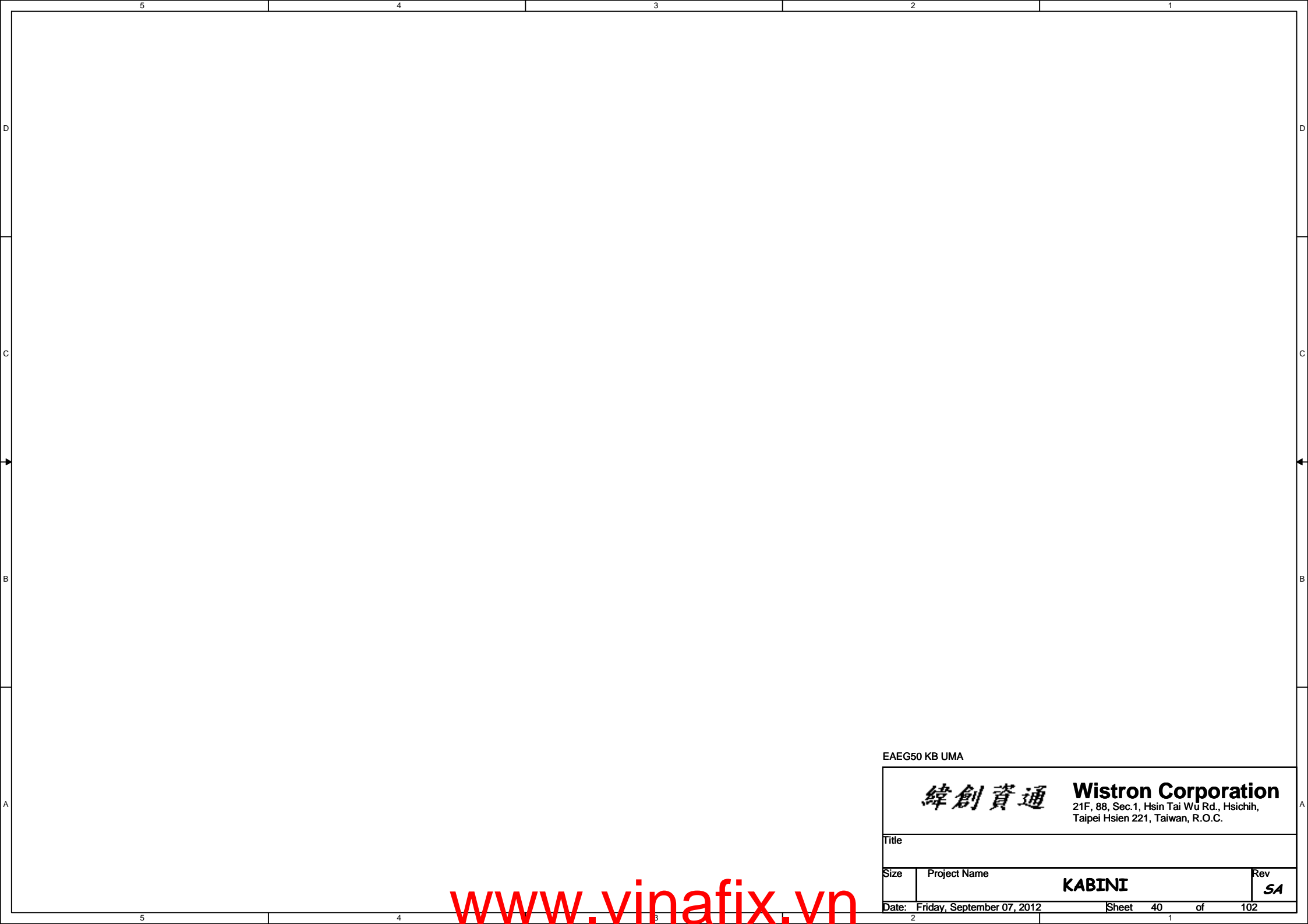
EAEG50 KB UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Deep Standby			
Size	Project Name		Rev
	KABINI		SA
Date: Friday, September 07, 2012		Sheet 38 of 102	



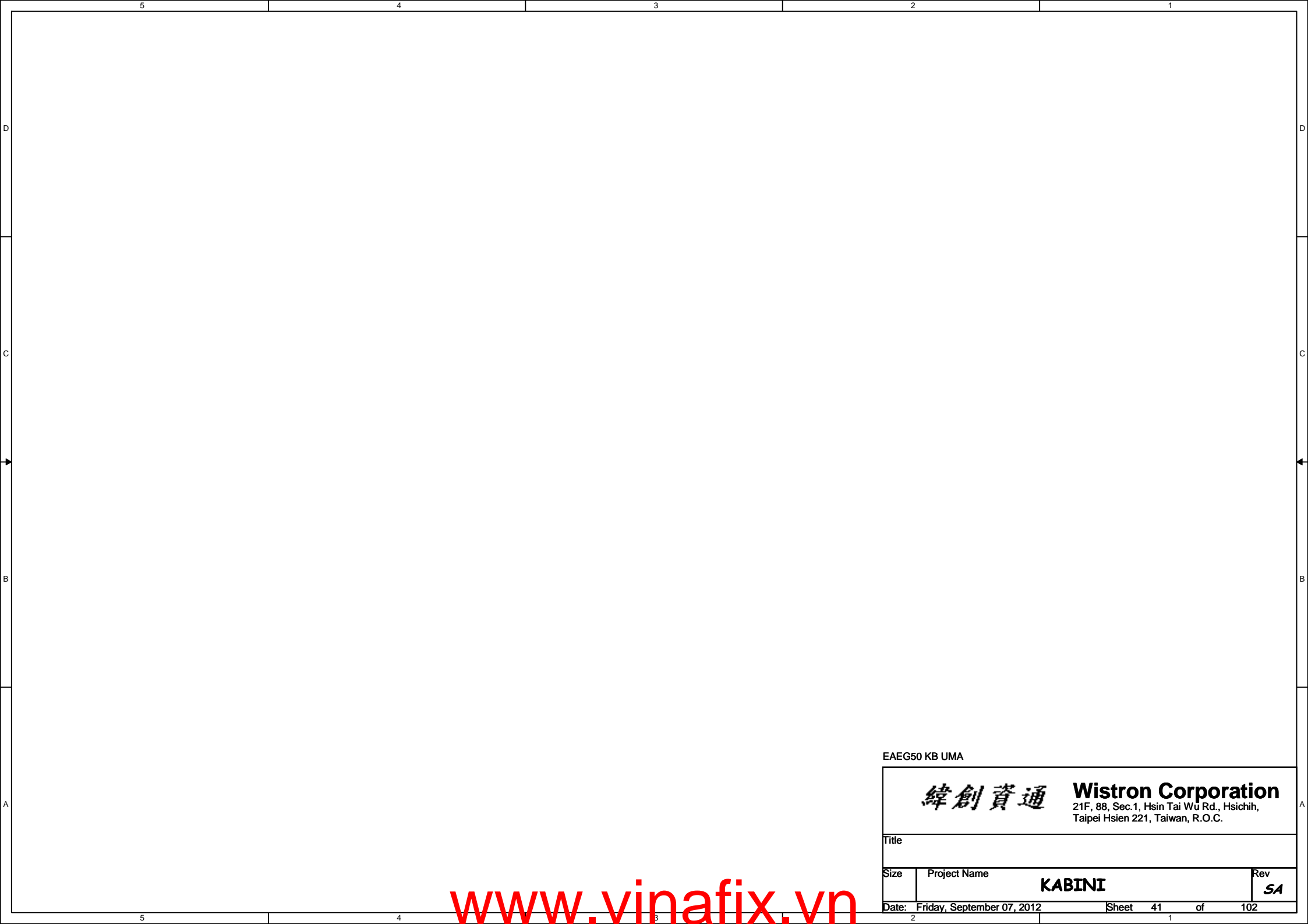
EAEG50 KB UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
1D05_M			
Size	Project Name		Rev
	KABINI		SA
Date: Friday, September 07, 2012		Sheet	39 of 102



EAEG50 KB UMA

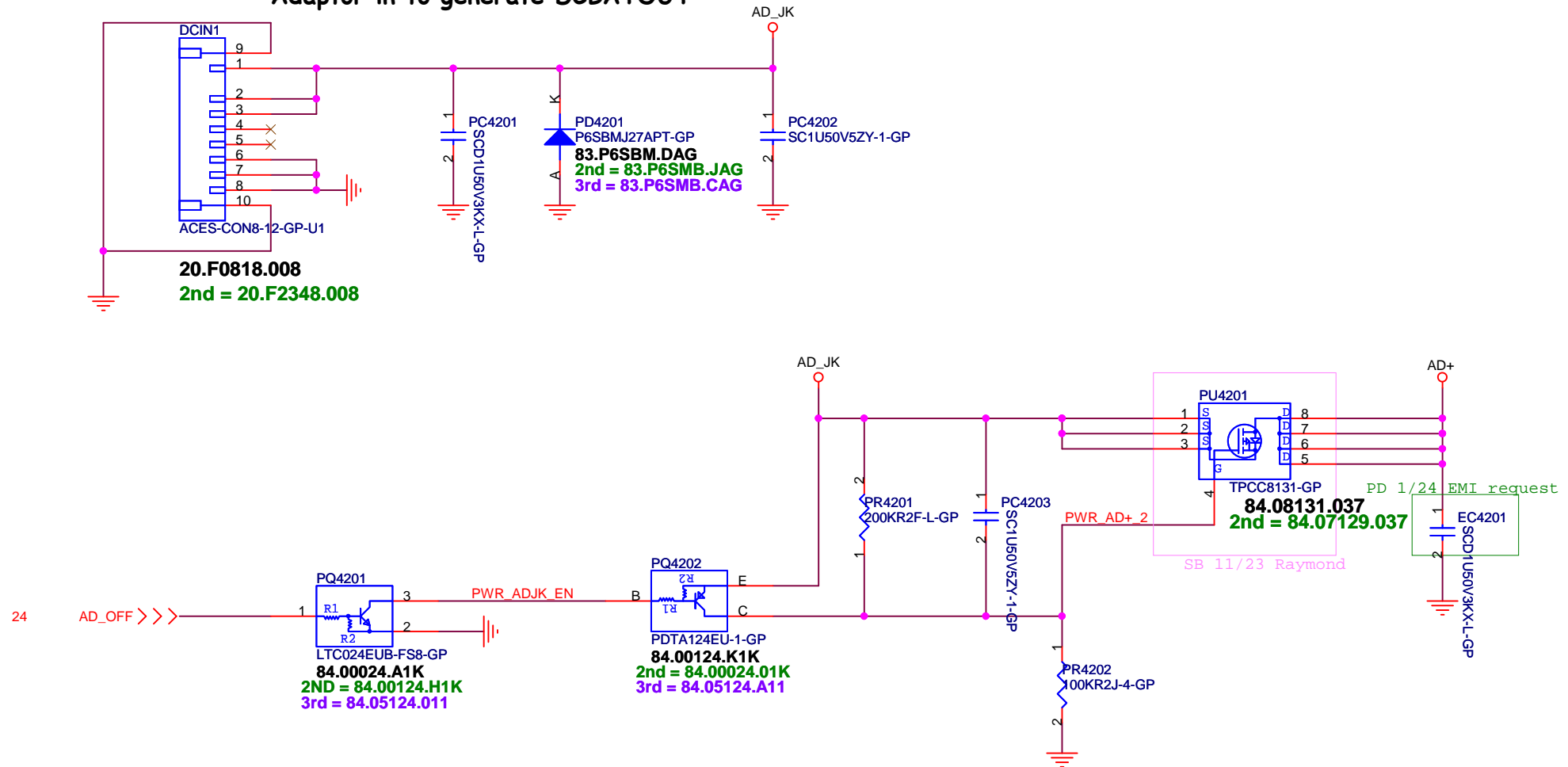
<div><div>緯創資通</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
Size	Project Name	Rev
	KABINI	SA
Date:	Friday, September 07, 2012	Sheet 40 of 102



EAEG50 KB UMA

<div><div>緯創資通</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
Size	Project Name	Rev
	KABINI	SA
Date:	Friday, September 07, 2012	Sheet 41 of 102

Adaptor in to generate DCBATOUT



EAEG50 KB UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DCIN JACK

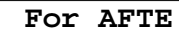
Size	Project Name
------	--------------

KABINI

Rev
SA

Date: Tuesday, February 19, 2013

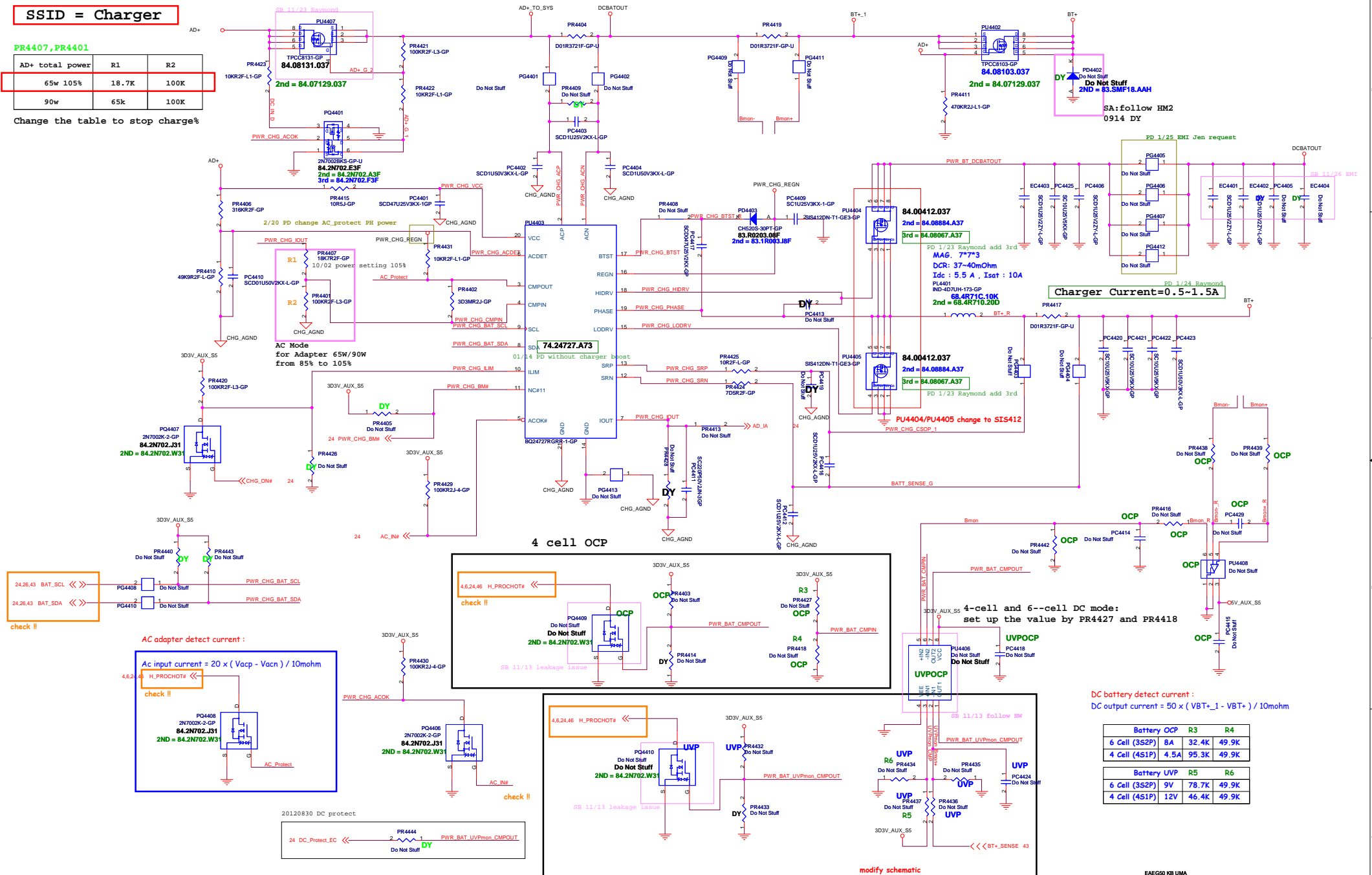
Sheet 42 of 102



PR4407,PR4401

AD+ total power	R1	R2
65w 105%	18.7K	100K
90w	65k	100K

Change the table to stop charge%



4 cell UVP

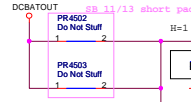
SSID = PWR.Plane.Regulator_3p3v5v

Cut off itself

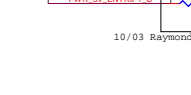
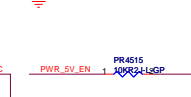
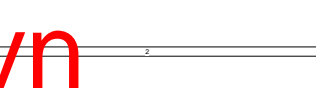
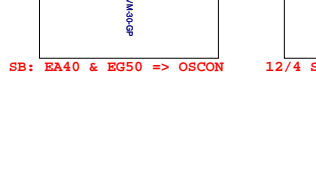
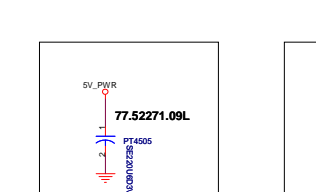
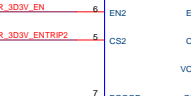
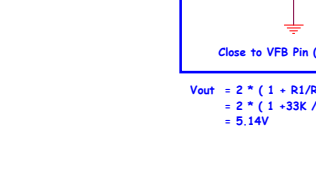
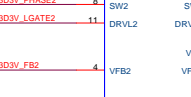
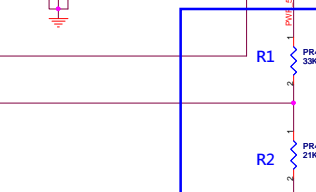
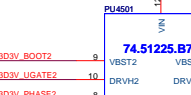
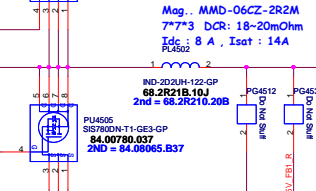
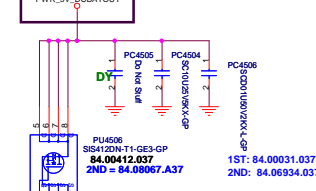
check (UVP)

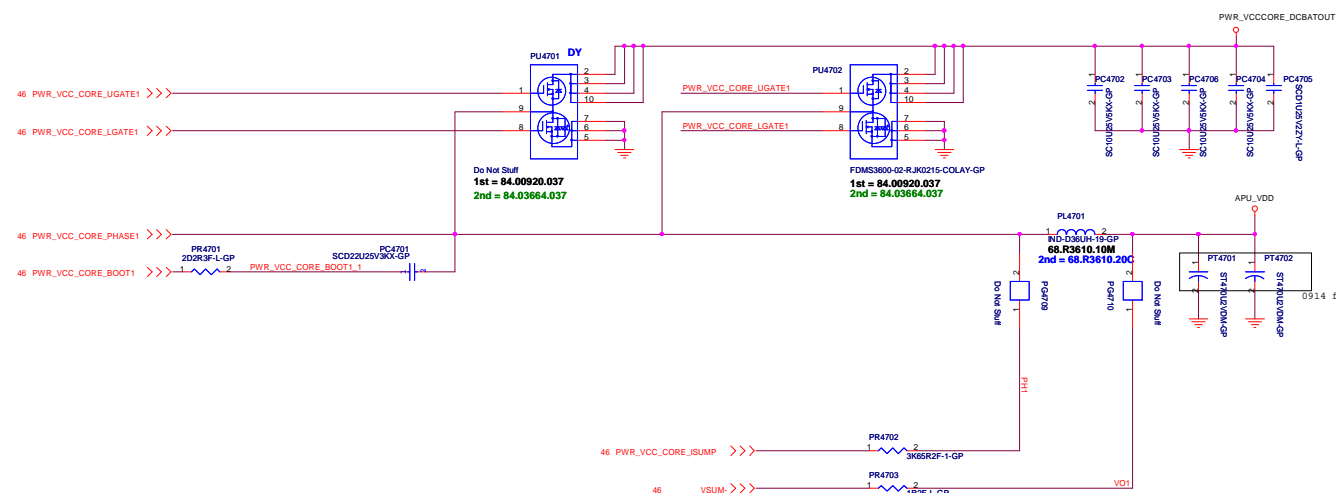
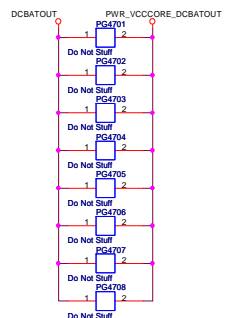
check (DCBATOUT)

check (DCBATOUT)

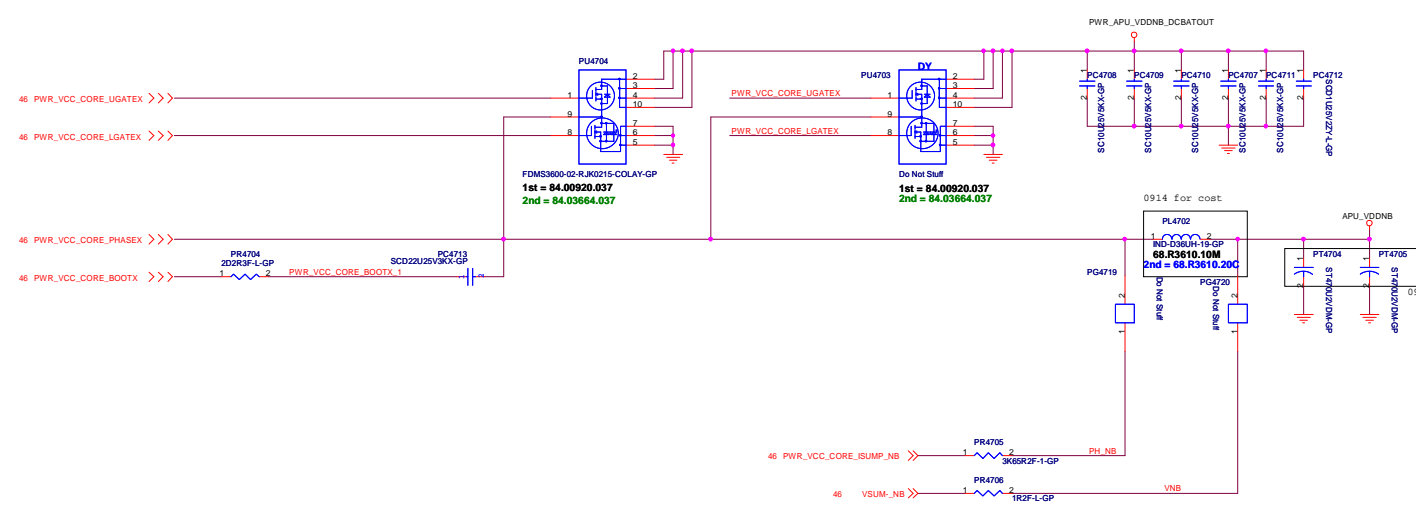
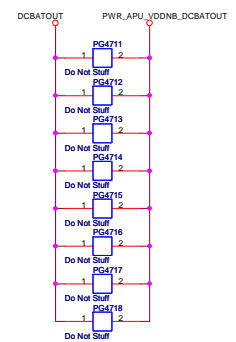


check (DCBATOUT)

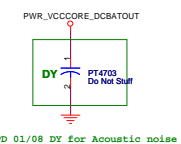




Iccmax=21A
TDC=16.8A
OCP>26.3A



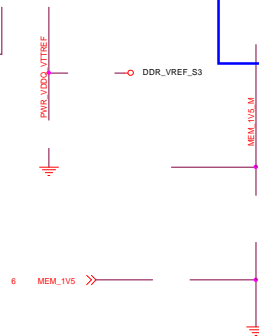
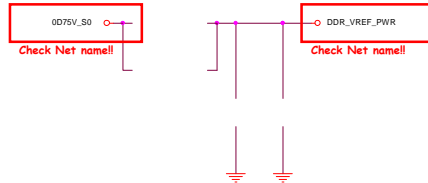
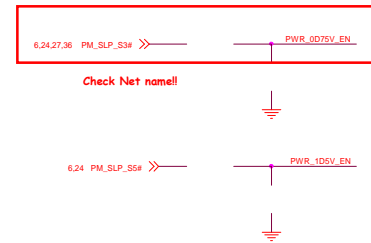
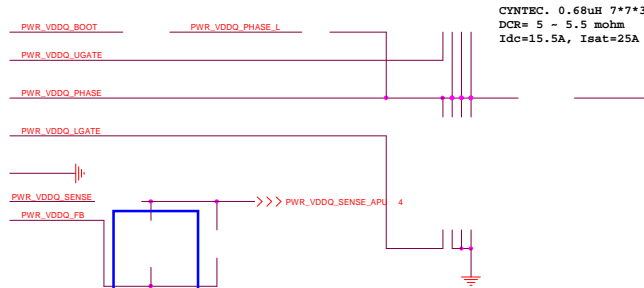
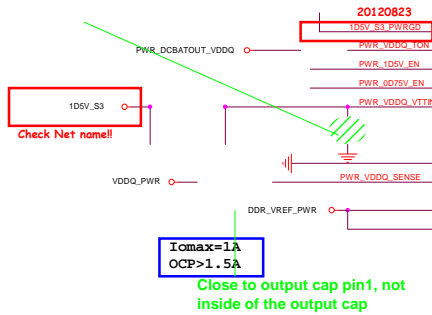
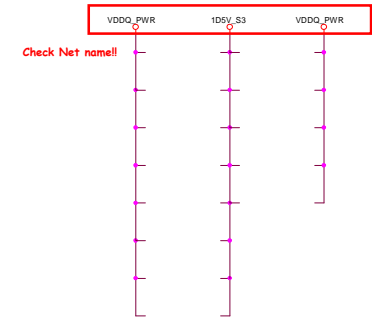
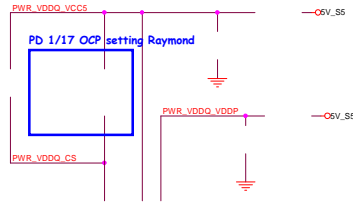
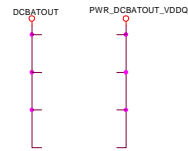
Iccmax=17A
TDC=13.6A
OCP>21.3A



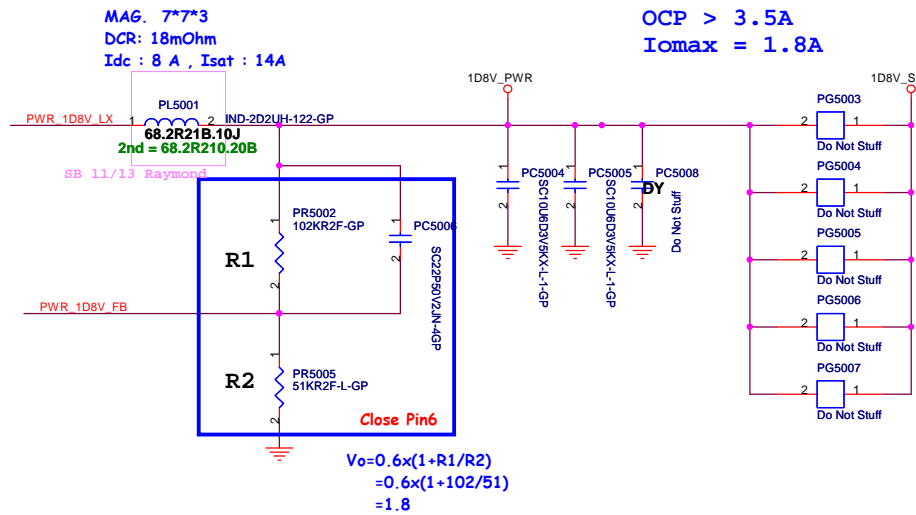
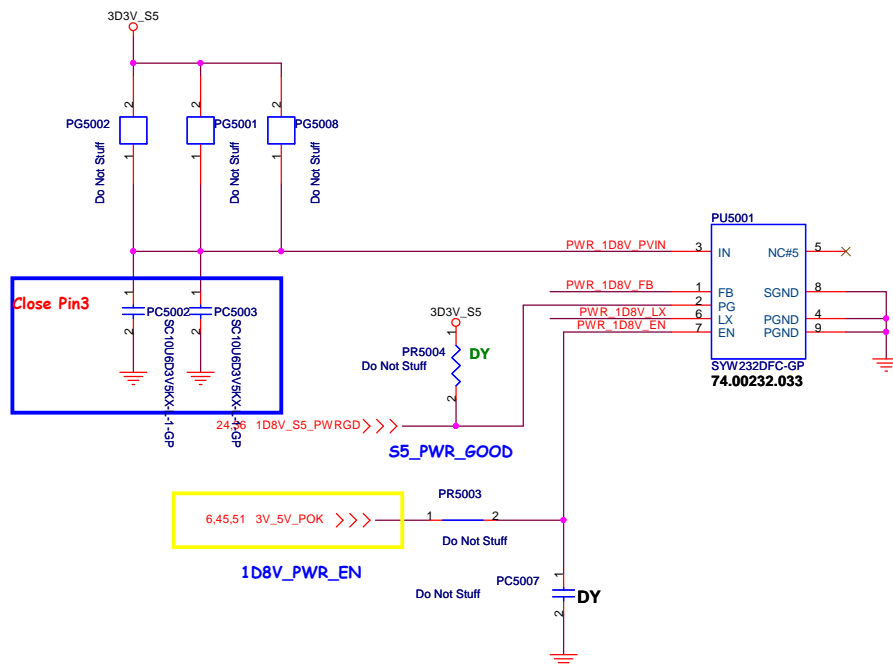
PD 01/08 DY for Acoustic noise

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```
SSID = PWR.Plane.Regulator_1p8v
```



EAEG50 KB UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

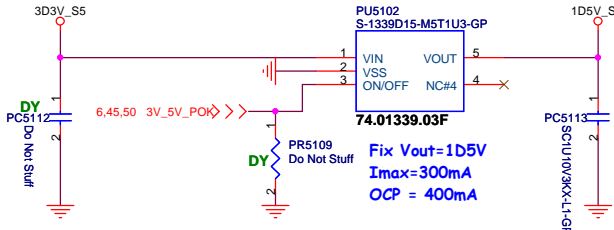
Title	1D8V_S0 SYW232
-------	----------------

Size A3	Document Number KABINI	Rev
------------	----------------------------------	-----

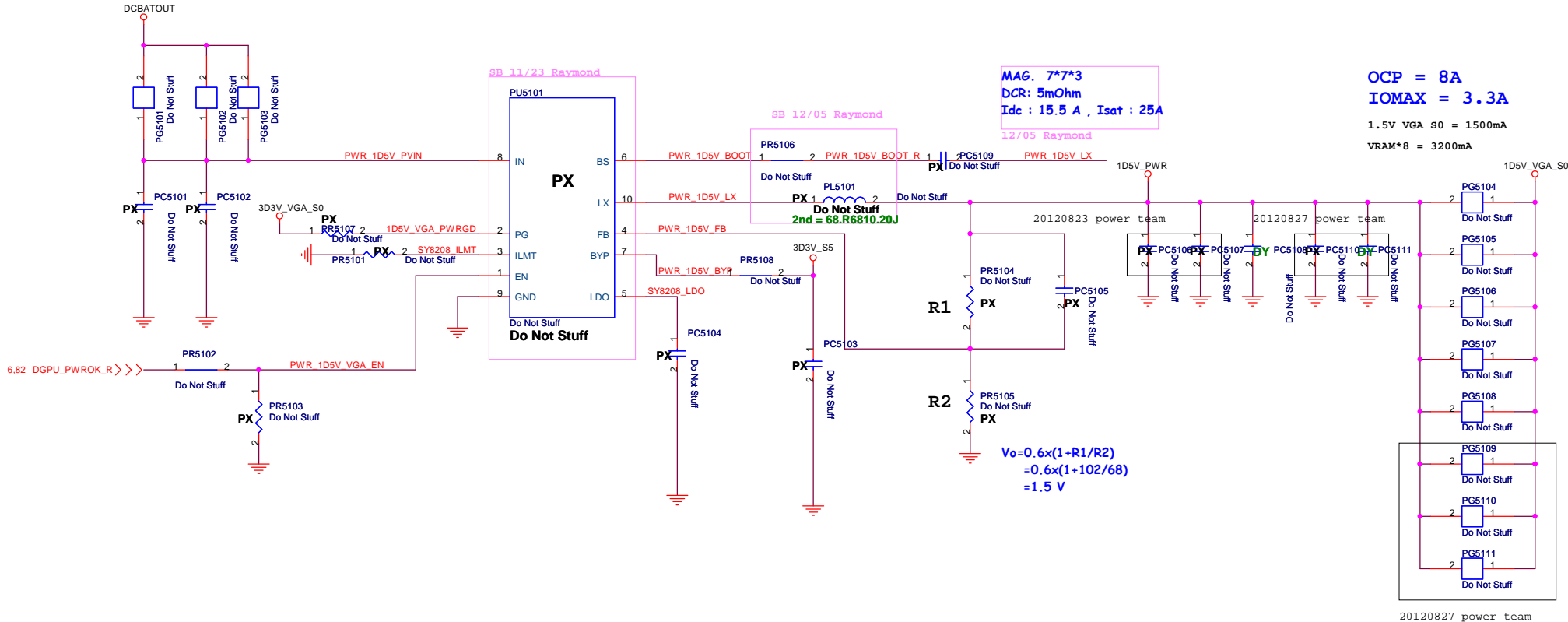
Date: Monday, February 04, 2013 Sheet 50 of 102

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LDO for 1D5V_S5 (SB 11/13)

$$1.5V \text{ S0} = 100mA(VDDIO_AZ) + 100mA(Audio) + 600mA(Minicard \text{ DY}) = 200mA$$


SY8208D for 1D5V_VGA_S0 (SB 11/13)



EAEG50 KB UMA

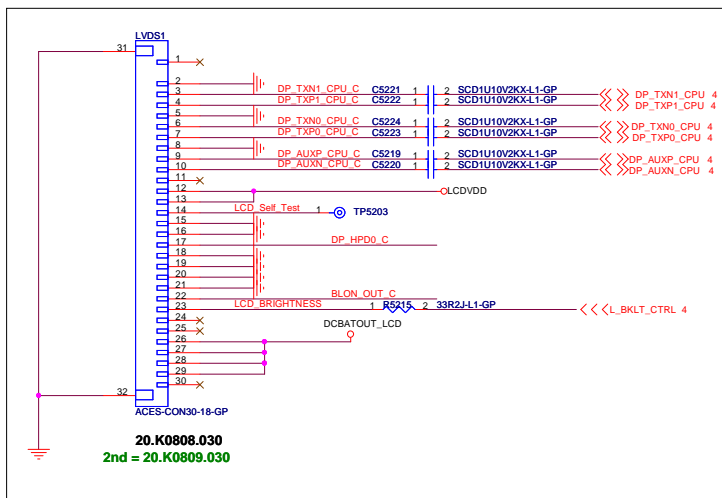
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	1D5V S5 SY8208D
-------	------------------------

Size A3	Document Number KABINI	Rev
Date: Tuesday, February 19, 2013	Sheet 51 of 102	

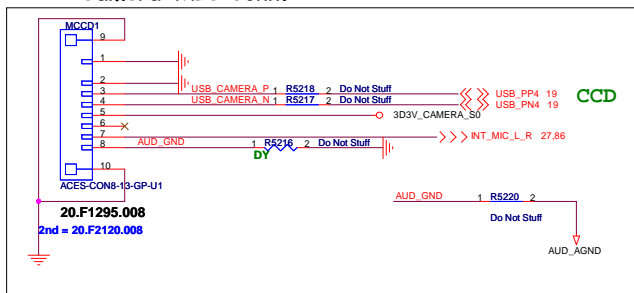
SSID = VIDEO

eDP Conn.



10/04 change to 20.K0808.030 for ME request

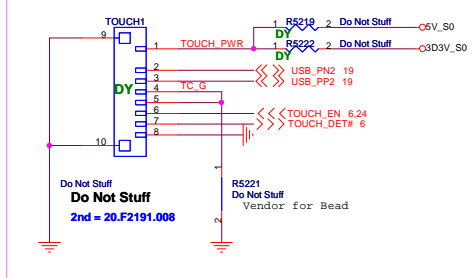
Camera+MIC Conn.



10/03 change to 8pin for del DMIC

10/15 change to 20.F1295.008 follow HW

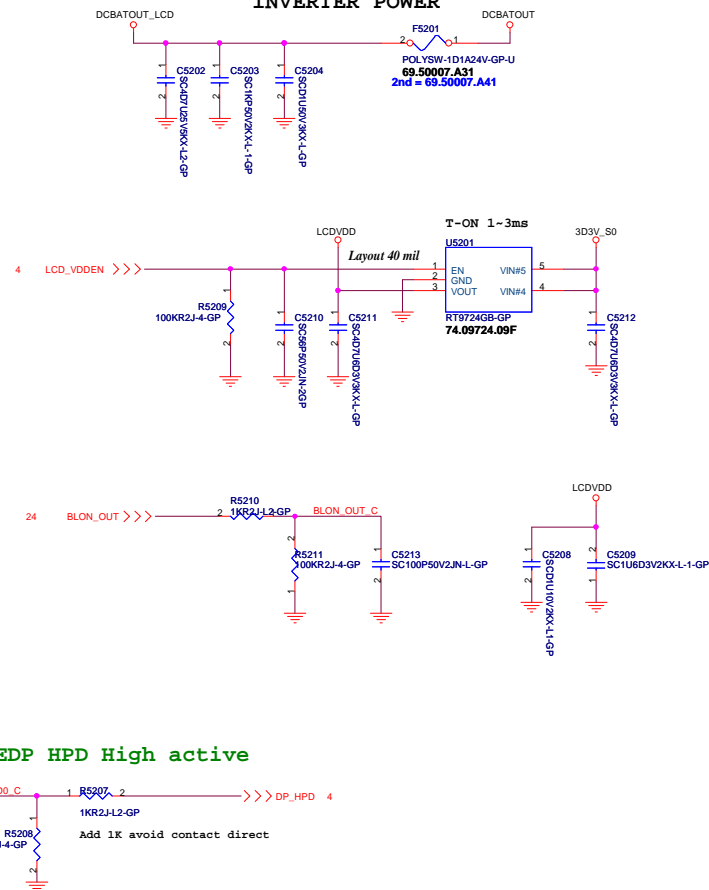
Touch Conn.



SB 12/12 DUMMY for ME issue

SC NO support

INVERTER POWER



86 AUD_GND <<<

86 DP_HP00_C >>>

86 BLON_OUT_C >>>

86 LCD_BRIGHTNESS >>>

86 DP_TXN1_CPU_C >>>

86 DP_TXP1_CPU_C >>>

86 DP_TXN0_CPU_C >>>

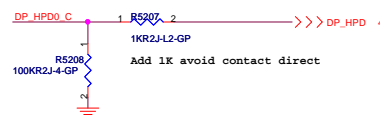
86 DP_TXP0_CPU_C >>>

86 DP_AUXP_CPU_C <<<

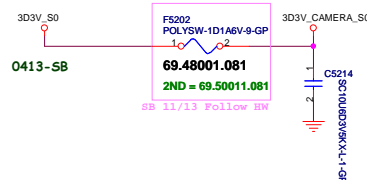
86 DP_AUXN_CPU_C <<<

For AFTE

EDP HPD High active



Camera Power

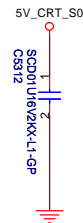
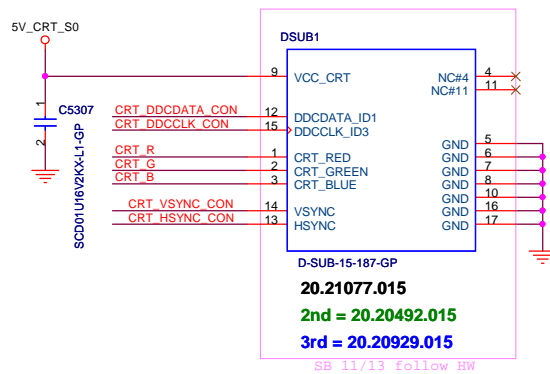


EAEG50 KB UMA

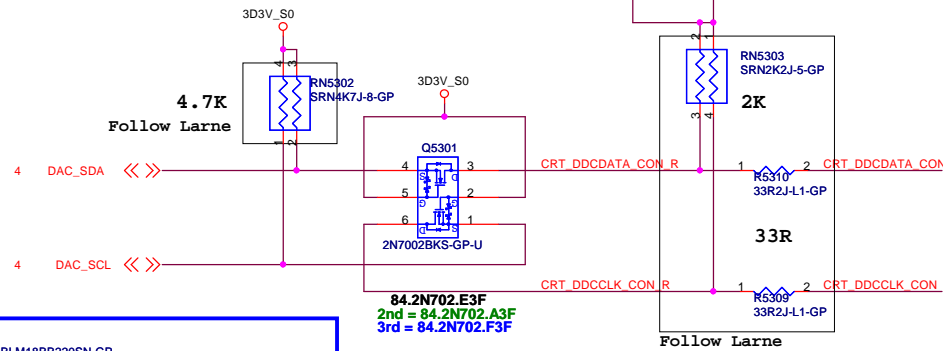
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

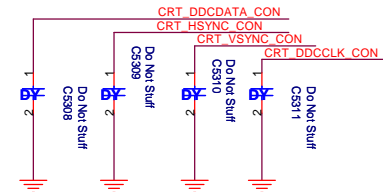
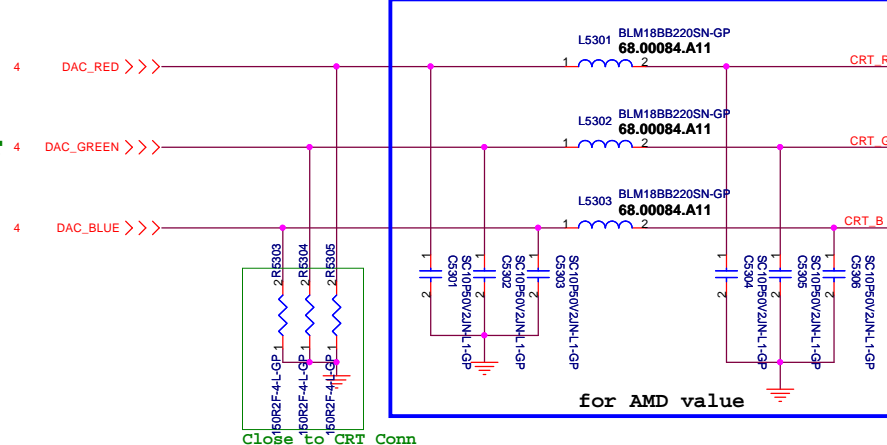
Title		
LCD Connector		
Size	Project Name	Rev
	KABINI	SA
Date: Monday, February 25, 2013		
Sheet 52 of 102		



CRT DDCDATA & DDCCLK level shift

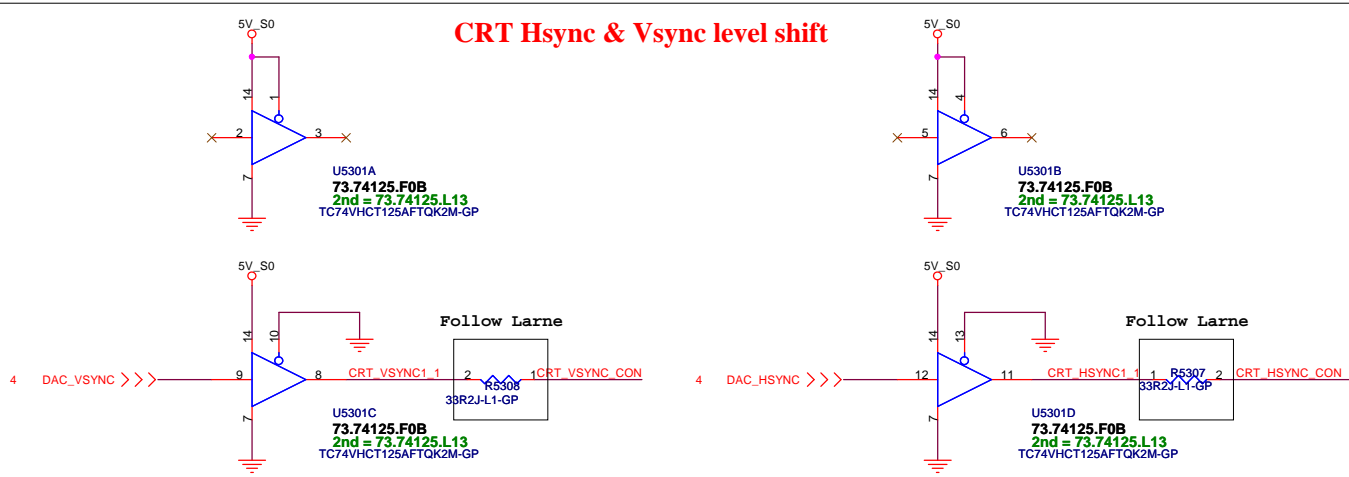


APU to CRT



10/16 follow COMAL

CRT Hsync & Vsync level shift



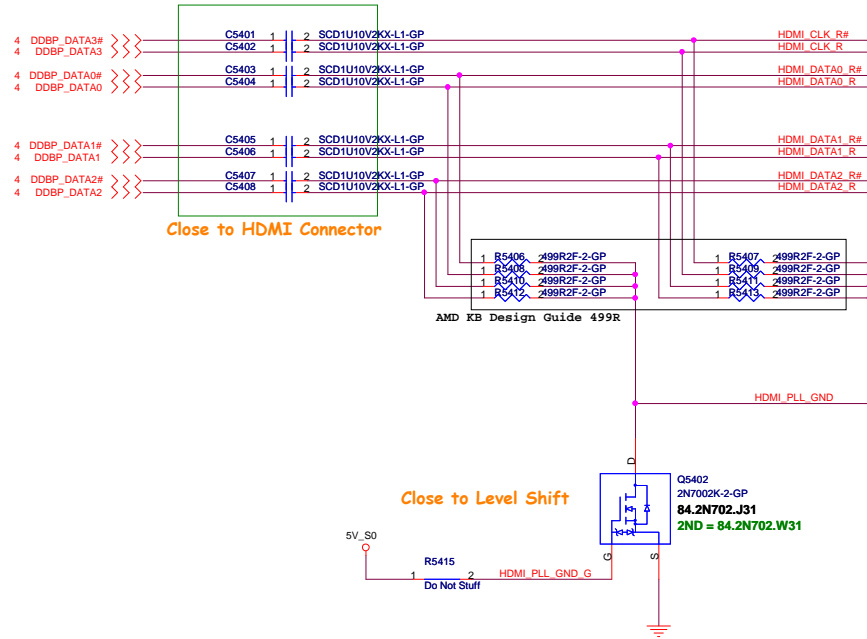
EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

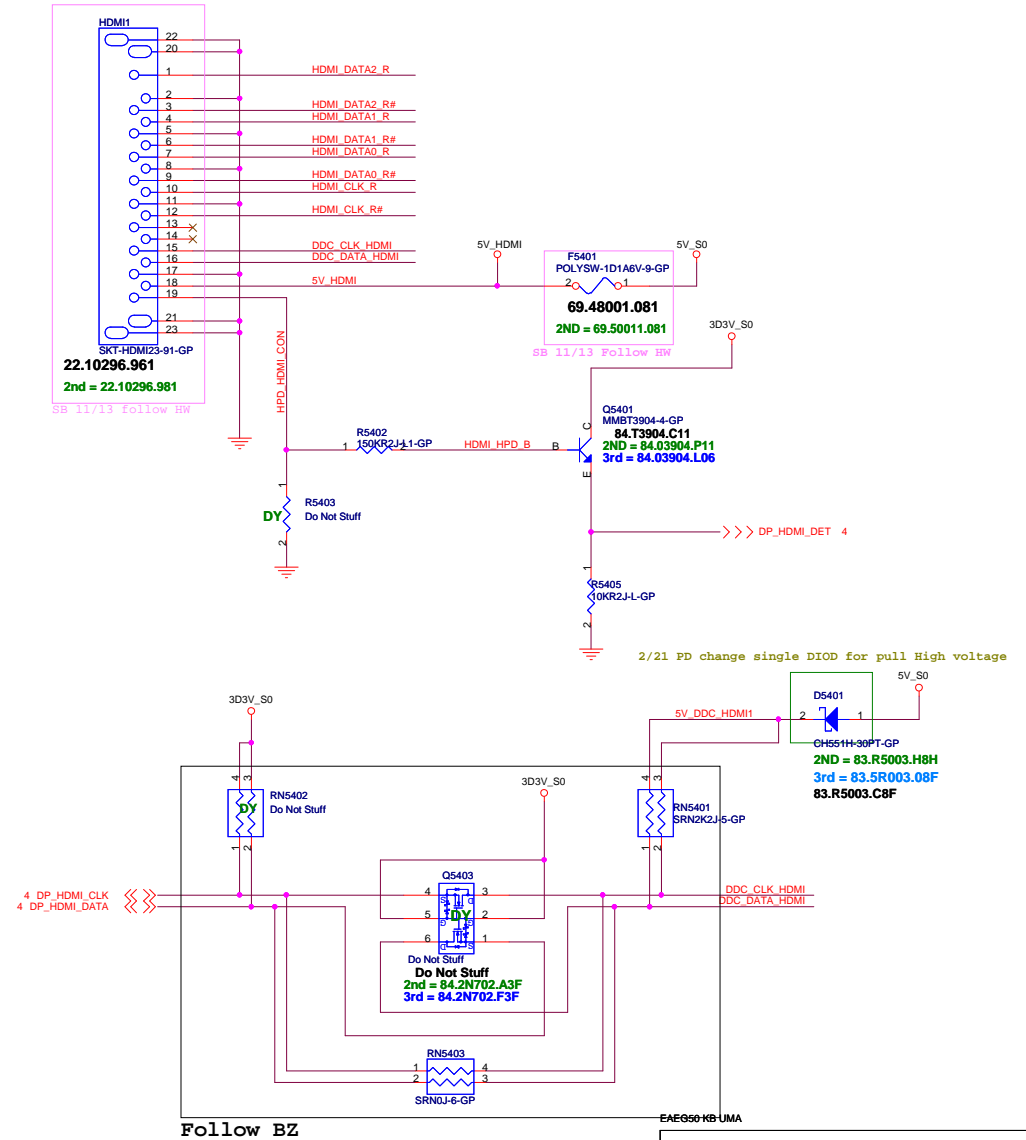
CRT Board Connector			
Title	Project Name		
Size	KABINI		
Date	Monday, February 04, 2013		
Sheet	53	of	102
Rev	SA		

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

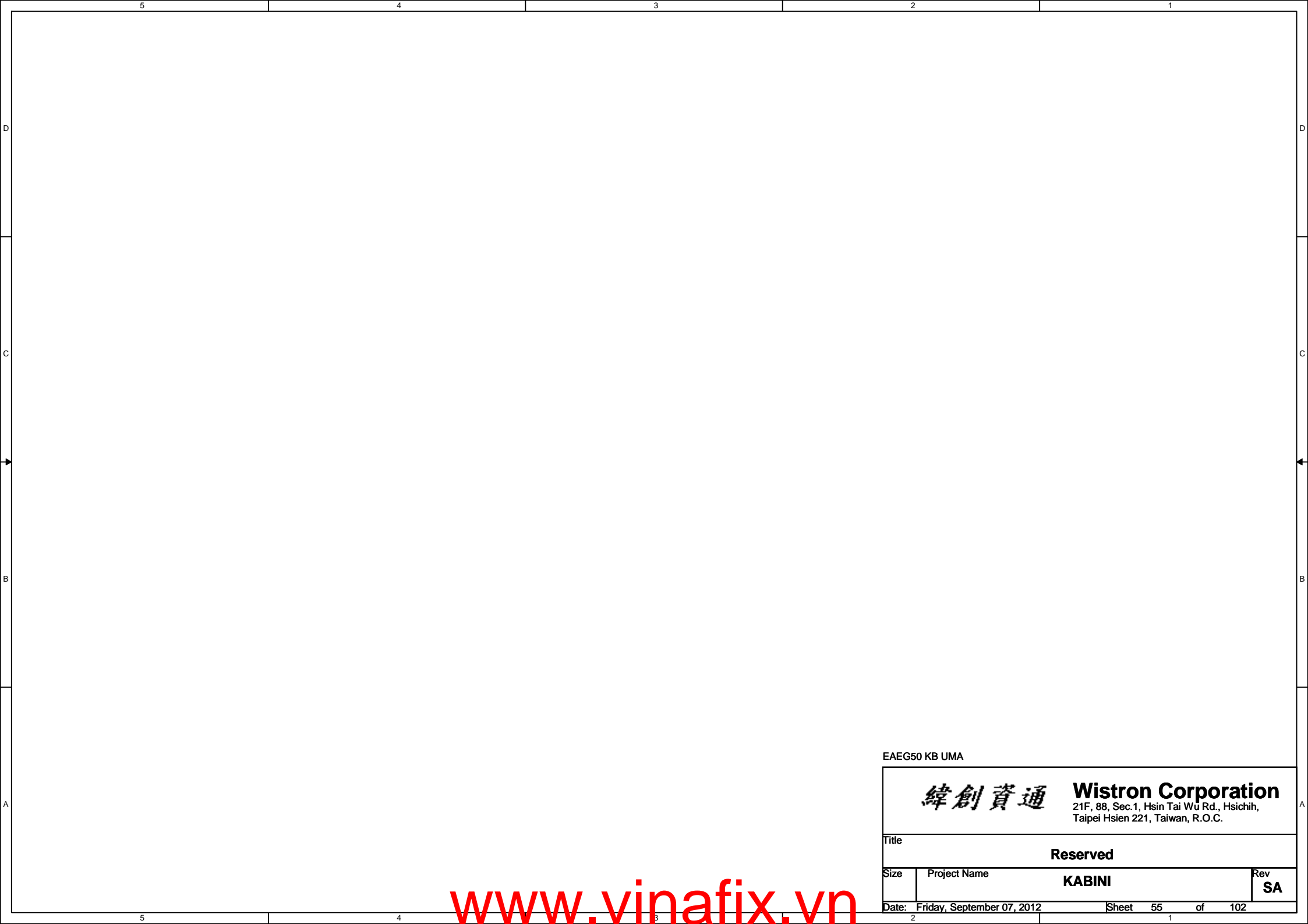


HDMI CONN



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HDMI Level Shifter/Connector			
Size	Project Name	KABINI	Rev SA
Date: Thursday, February 21, 2013	Sheet	54	of 102



5

4

3

2

1

D

D

C

C

B

B

A

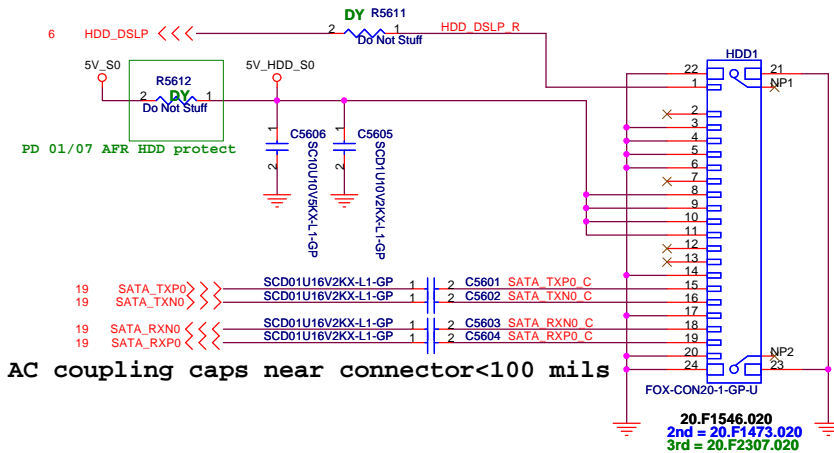
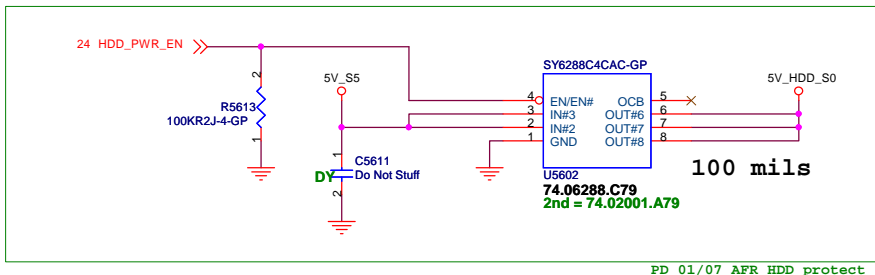
A

EAEG50 KB UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Project Name		Rev
	KABINI		SA
Date: Friday, September 07, 2012		Sheet	55 of 102

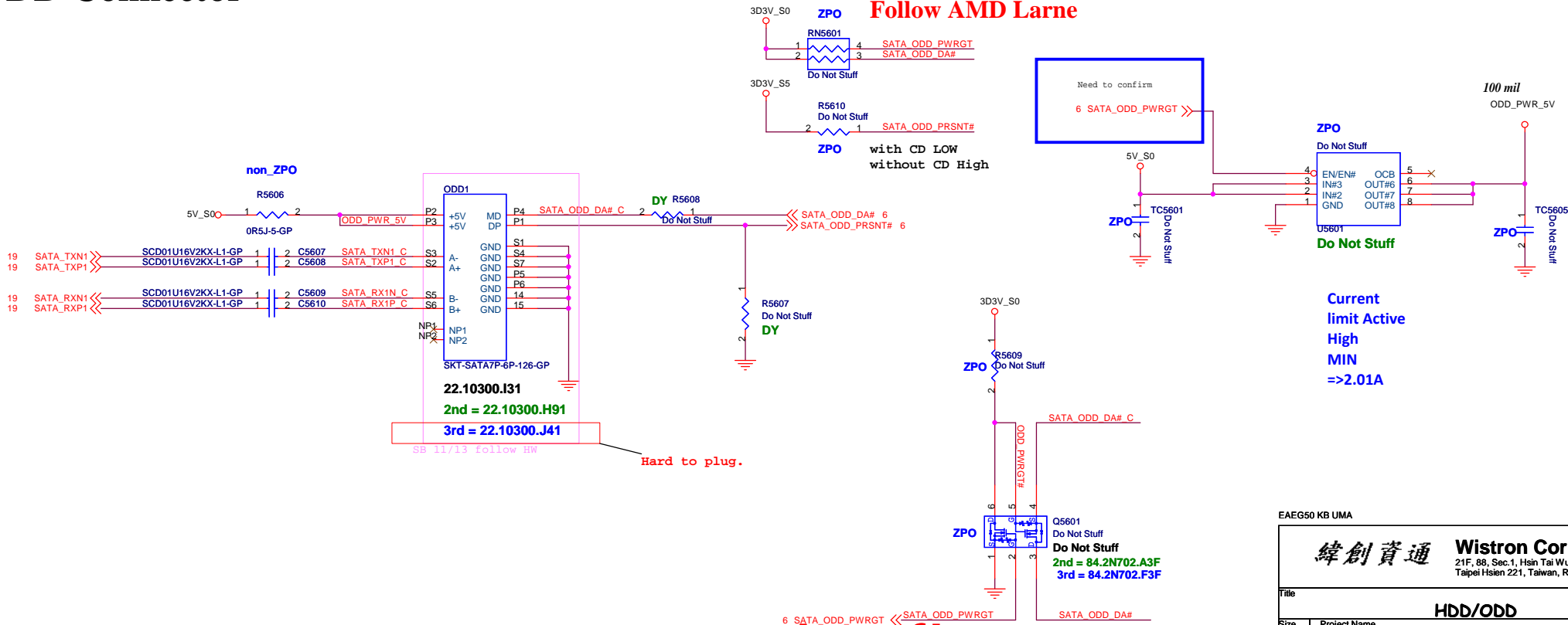
SSID = SATA

SATA HDD Connector



ODD Connector

SATA Zero Power ODD Follow AMD Larne



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Title

HDD/ODD

Size	Project Name
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[illegible]

KABINI

Rev

5

Date: Monday, February 04, 2013

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2	3
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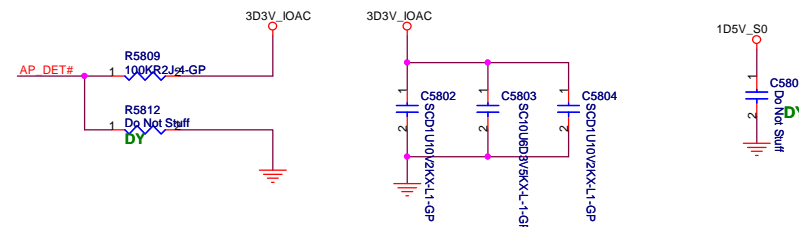
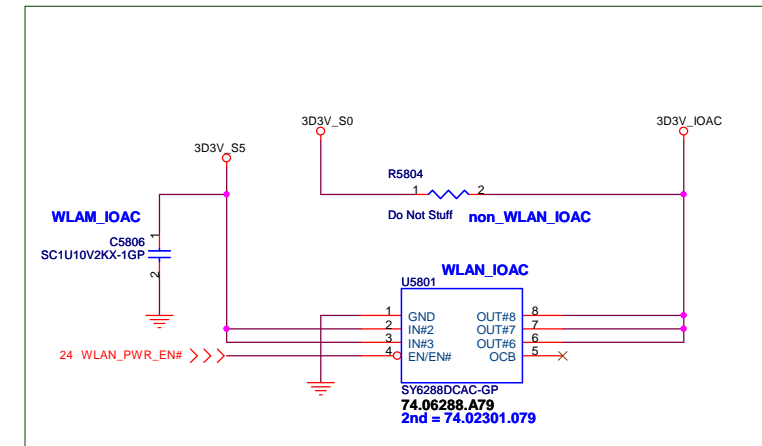
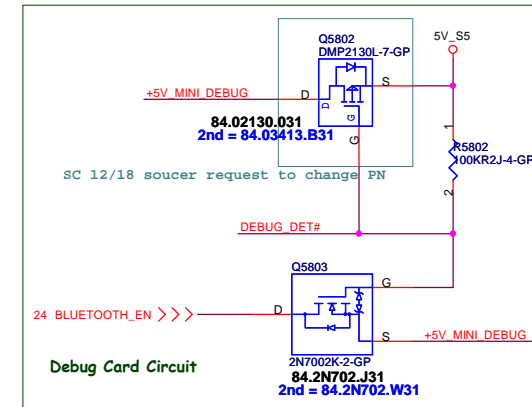
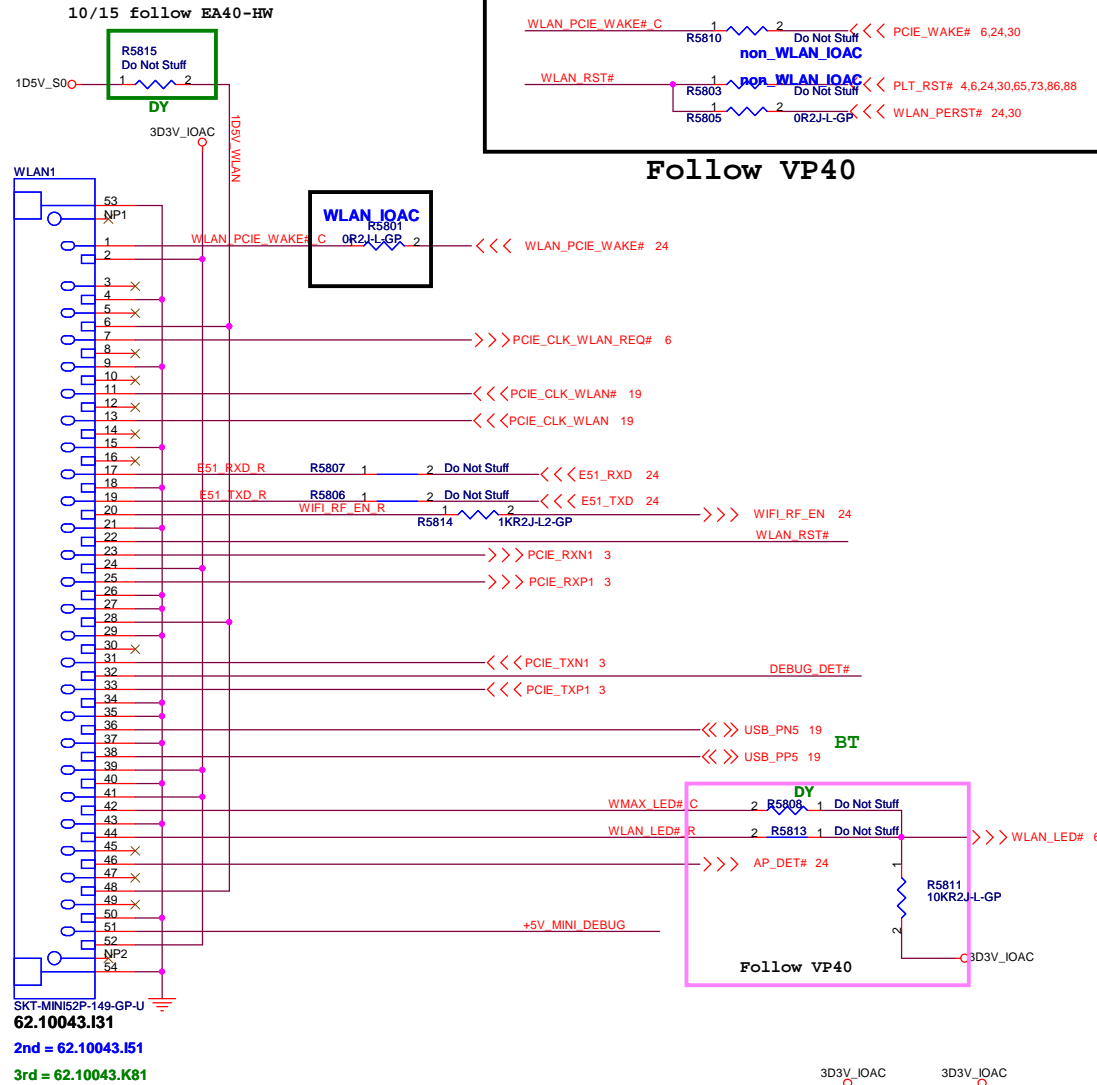


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Title					
Reserved					
Size	Project Name		Rev		
	KABINI		SA		
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2		1			

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



SSID = Wireless

Mini Card Connector(WWAN)

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Title

WWAN CONN

Size

Project Name

KABINI

Rev

SA

Date: Friday, September 07, 2012

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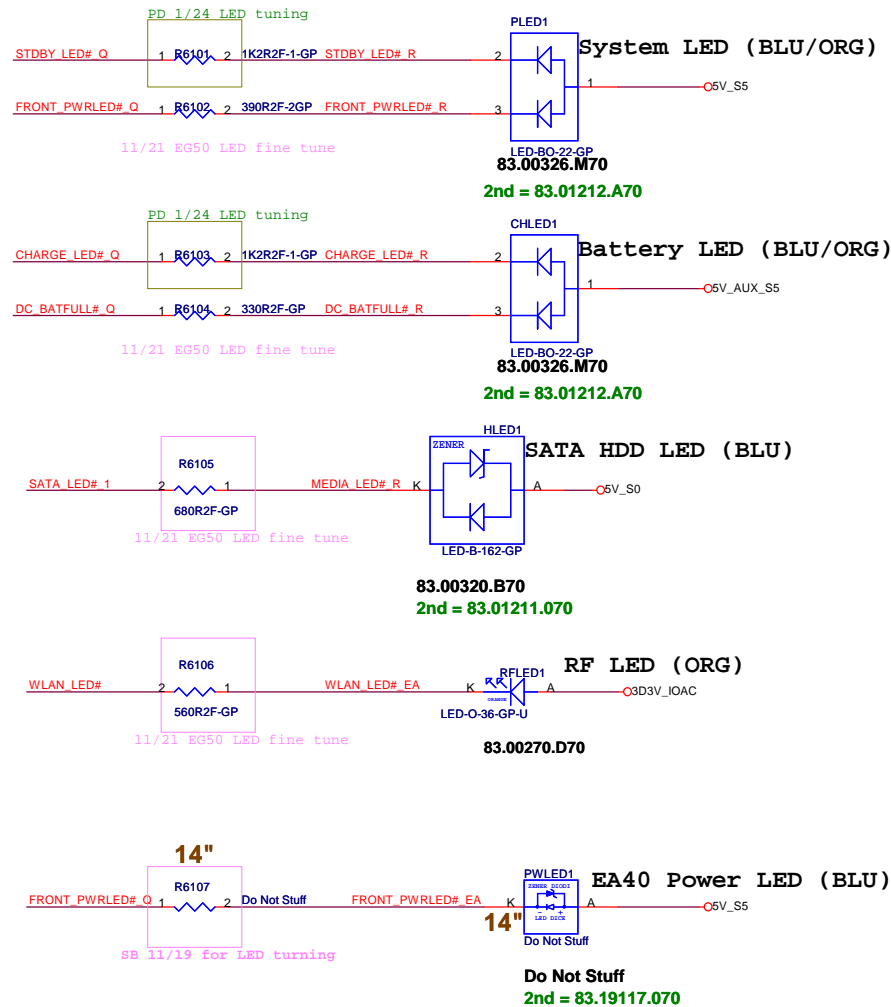
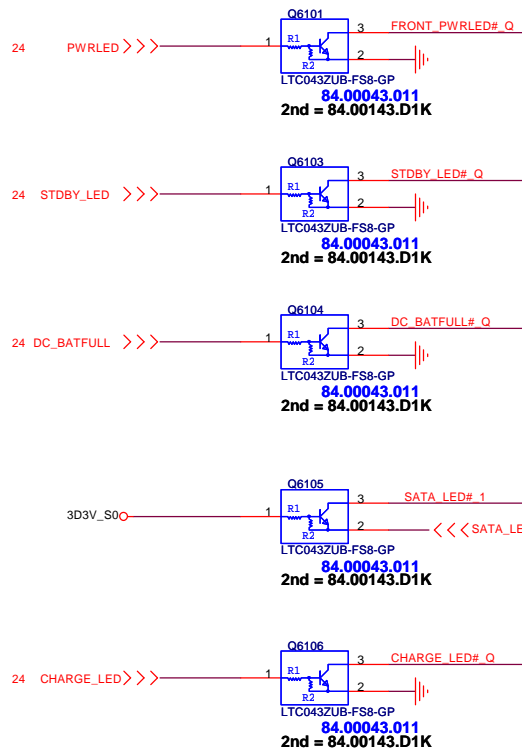
SSID = mSATA

Mini Card Connector(mSATA)

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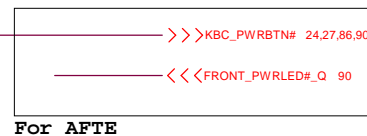
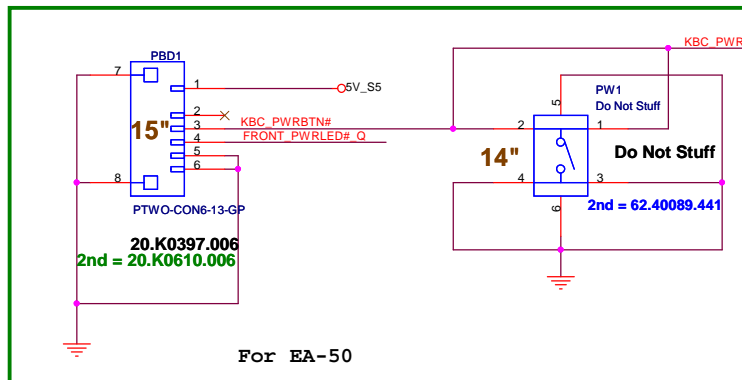
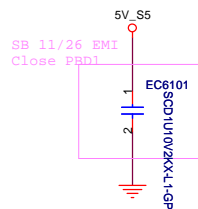
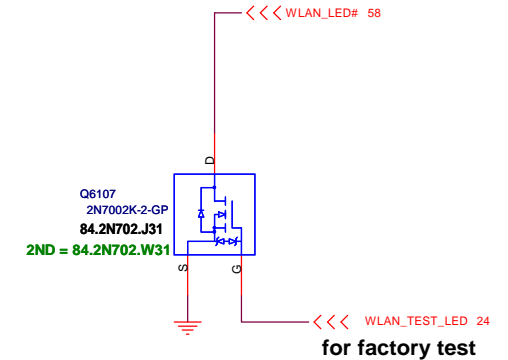
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title mSATA Connector		
Size	Project Name KABINI	Rev SA
Date: Friday, September 07, 2012		Sheet 60 of 102

SSID = User.Interface



WLAN_LED

From module



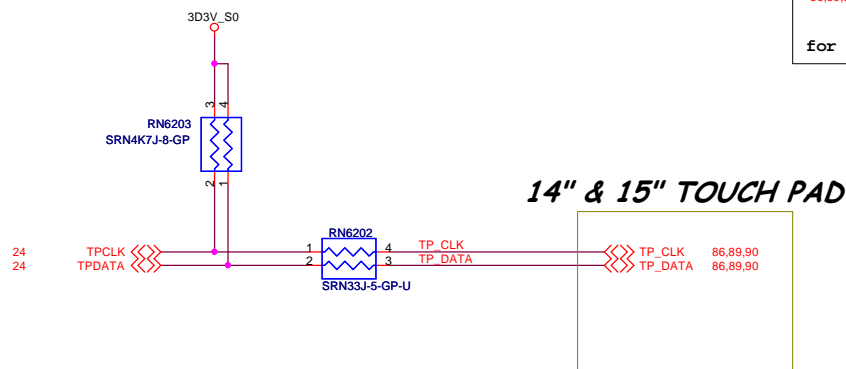
EAEG50 KB UMA

緯創資通 Wistron Corporation
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Title		
LED Bard/Power Button		
Size	Project Name	Rev
	KABINI	SA
Date:	Monday, February 04, 2013	Sheet 61 of 102

Internal KeyBoard Connector

for AFTP



PD 1/14 Diffferent 14" & 15" TOUCH PAD reversion

Diagram of the ACES-CON26-13-GP-U connector. The connector is a 26-pin D-sub connector. The pin assignments are as follows:

Pin	Signal Name
1	KCOL0
2	KCOL1
3	KCOL2
4	KCOL3
5	KCOL4
6	KCOL5
7	KCOL6
8	KCOL7
9	KCOL8
10	KCOL9
11	KCOL10
12	KCOL11
13	KCOL12
14	KCOL13
15	KCOL14
16	KCOL15
17	KCOL16
18	KCOL17
19	KROW0
20	KROW1
21	KROW2
22	KROW3
23	KROW4
24	KROW5
25	KROW6
26	KROW7

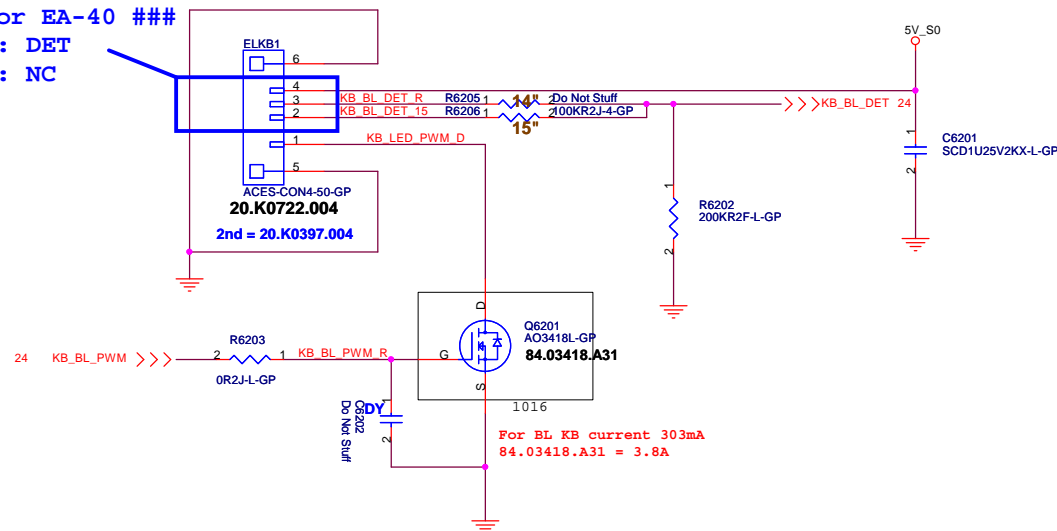
The diagram also shows the connector's physical dimensions and pin locations. The connector is labeled "KB1 ACES-CON26-13-GP-U". The pin locations are marked with "27" and "28". The connector is shown with a ground symbol on the right. The text "20.K0615.026" and "2nd = 20.K0449.026" is present. A legend at the bottom right shows a blue line and a red line, both labeled "KROW[0..7]".

————<<< KROW[0..7] 24,86

————>>> KCOL[0..17] 24,86

```
Pin3 : NC
Pin2 : DET
```

Pin3 : DET
Pin2 : NC



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Title

Key Board/Touch Pad

Size

	Project Name
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KABINI

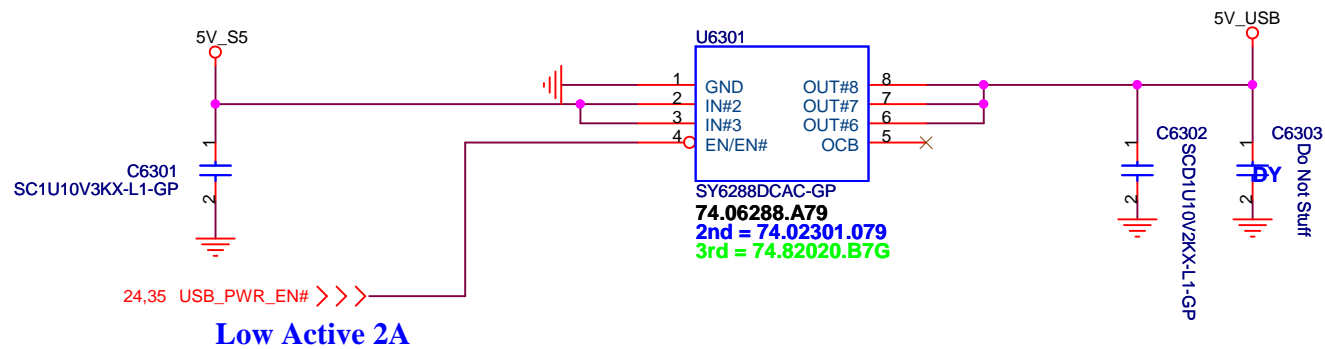
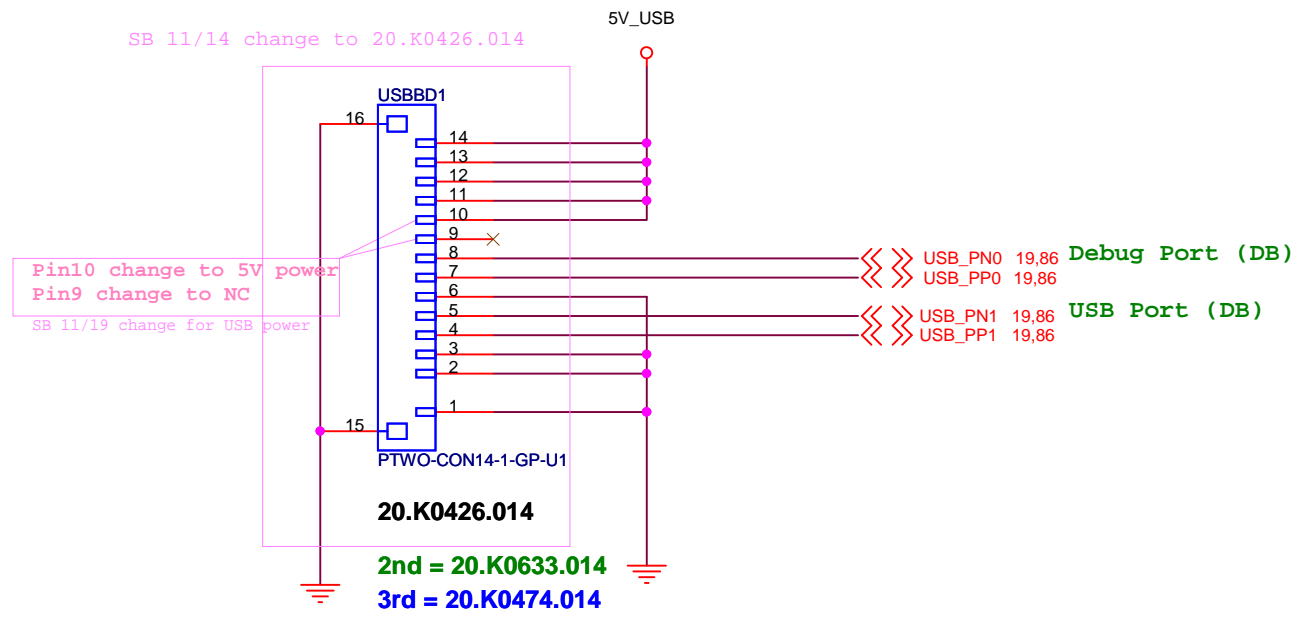
Rev

SA

Date: Tuesday, February 19, 2013

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Title

IO Board Connector

Size

Project Name

KABINI

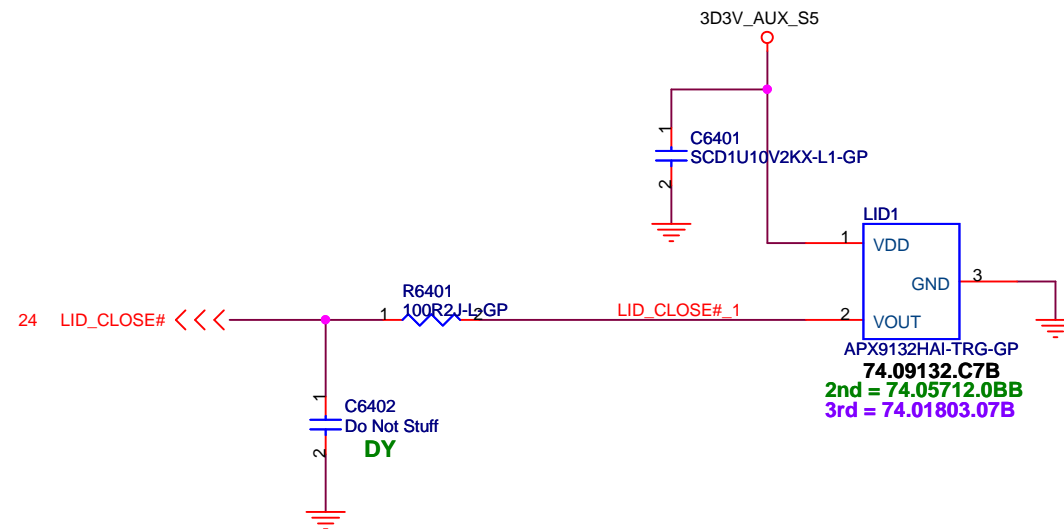
Rev

SA

Date: Monday, February 04, 2013

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Title

Hall Sensor

Size

Project Name

KABINI

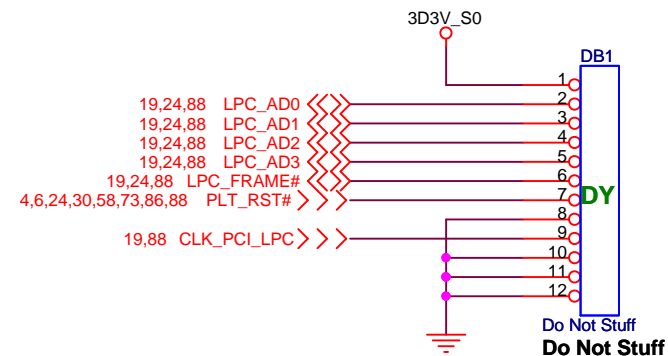
Rev

SA

Date: Monday, February 04, 2013

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Title

Dubug connector

Size

Project Name

KABINI

Rev

SA

Date: Monday, February 04, 2013

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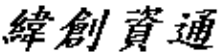
(Blanking)

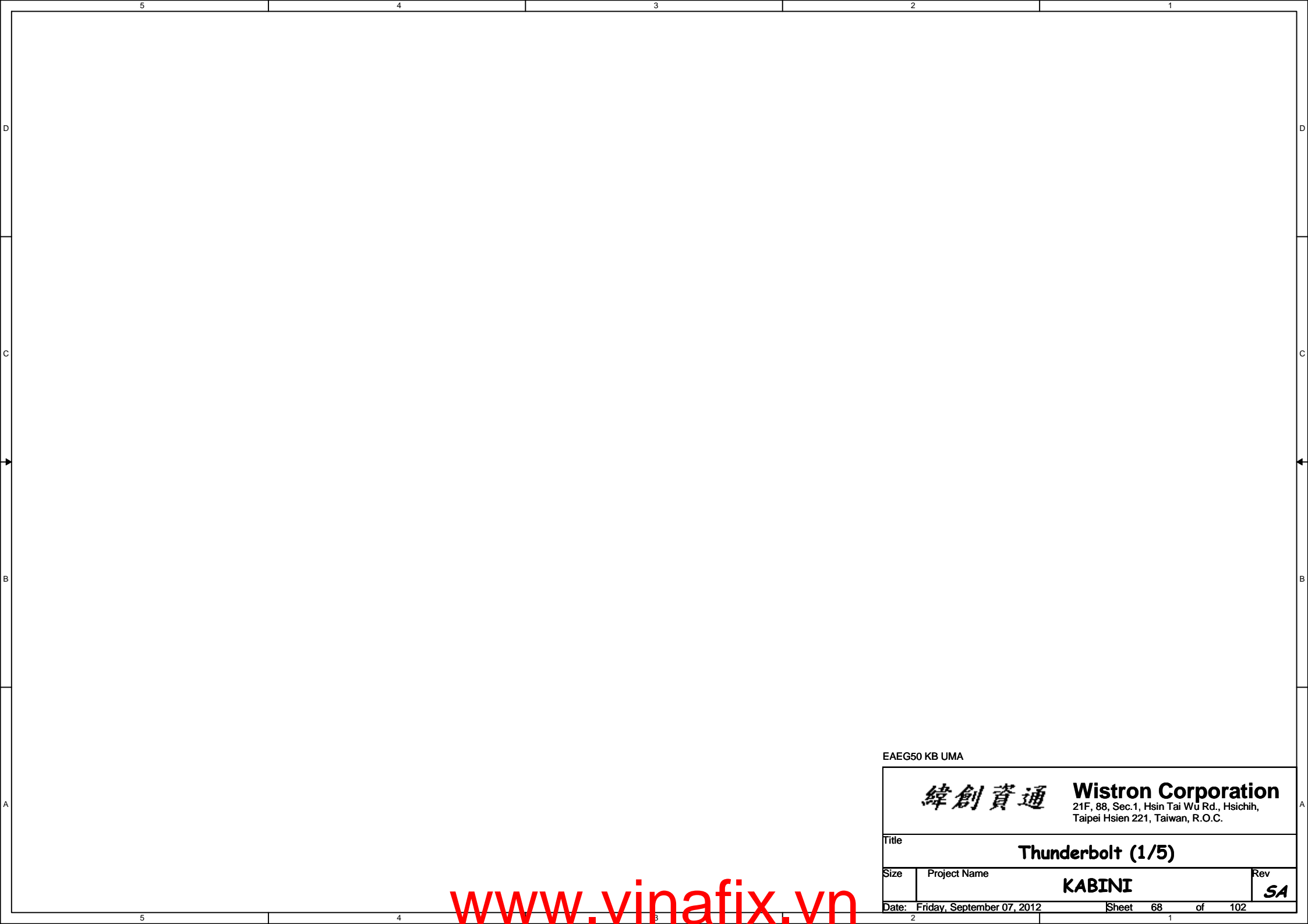
EAEG50 KB UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Project Name		Rev
	KABINI		SA
Date: Friday, September 07, 2012		Sheet 66 of 102	


SSID = User.Interface

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Title			
G Sensor			
Size	Project Name		Rev
	KABINI		SA
Date: Friday, September 07, 2012		Sheet	67 of 102




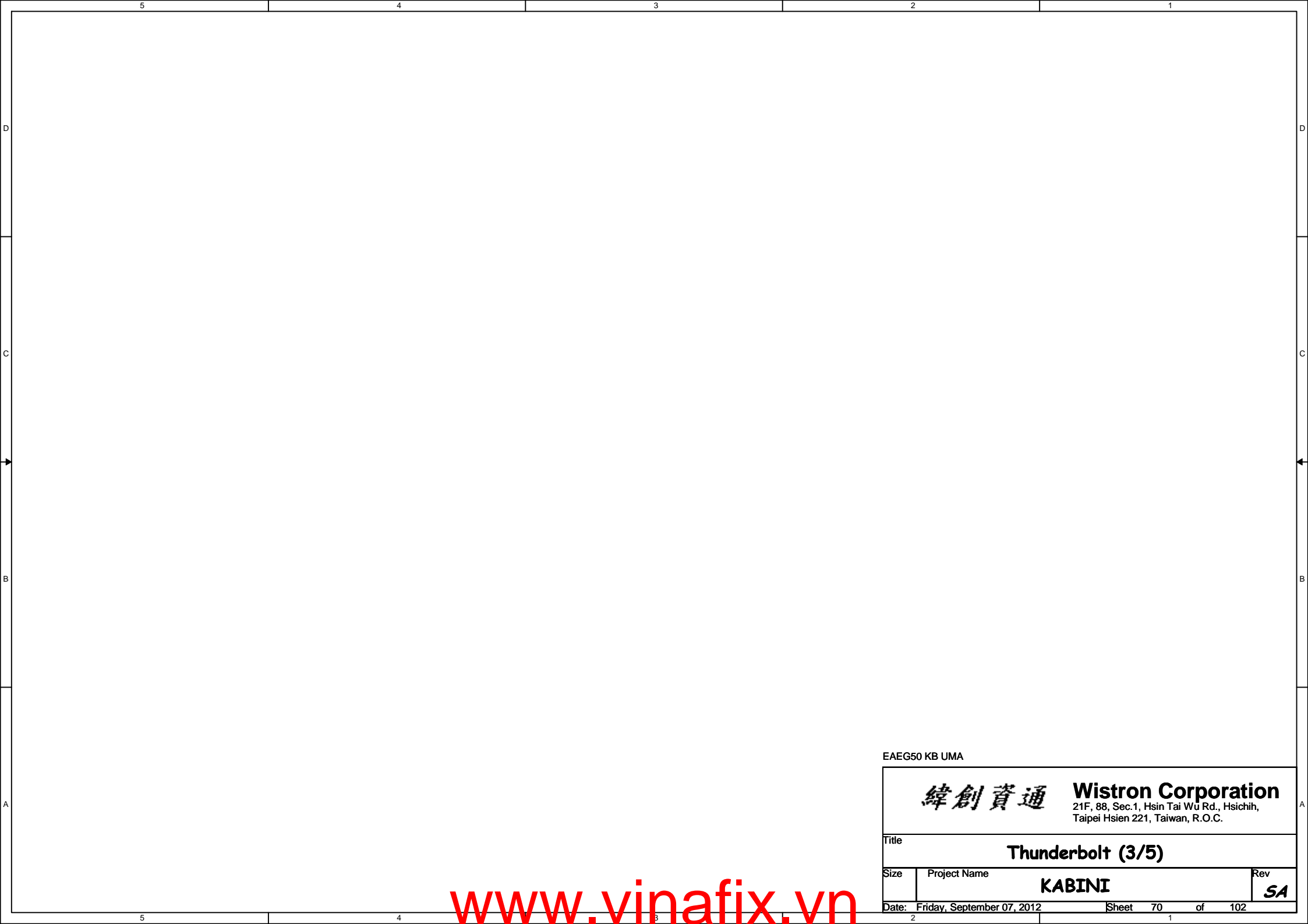
EAEG50 KB UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Thunderbolt (1/5)		
Size	Project Name KABINI	Rev SA
Date: Friday, September 07, 2012		Sheet 68 of 102



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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Thunderbolt (2/5)		
Size	Project Name KABINI	Rev SA
Date: Friday, September 07, 2012		Sheet 69 of 102



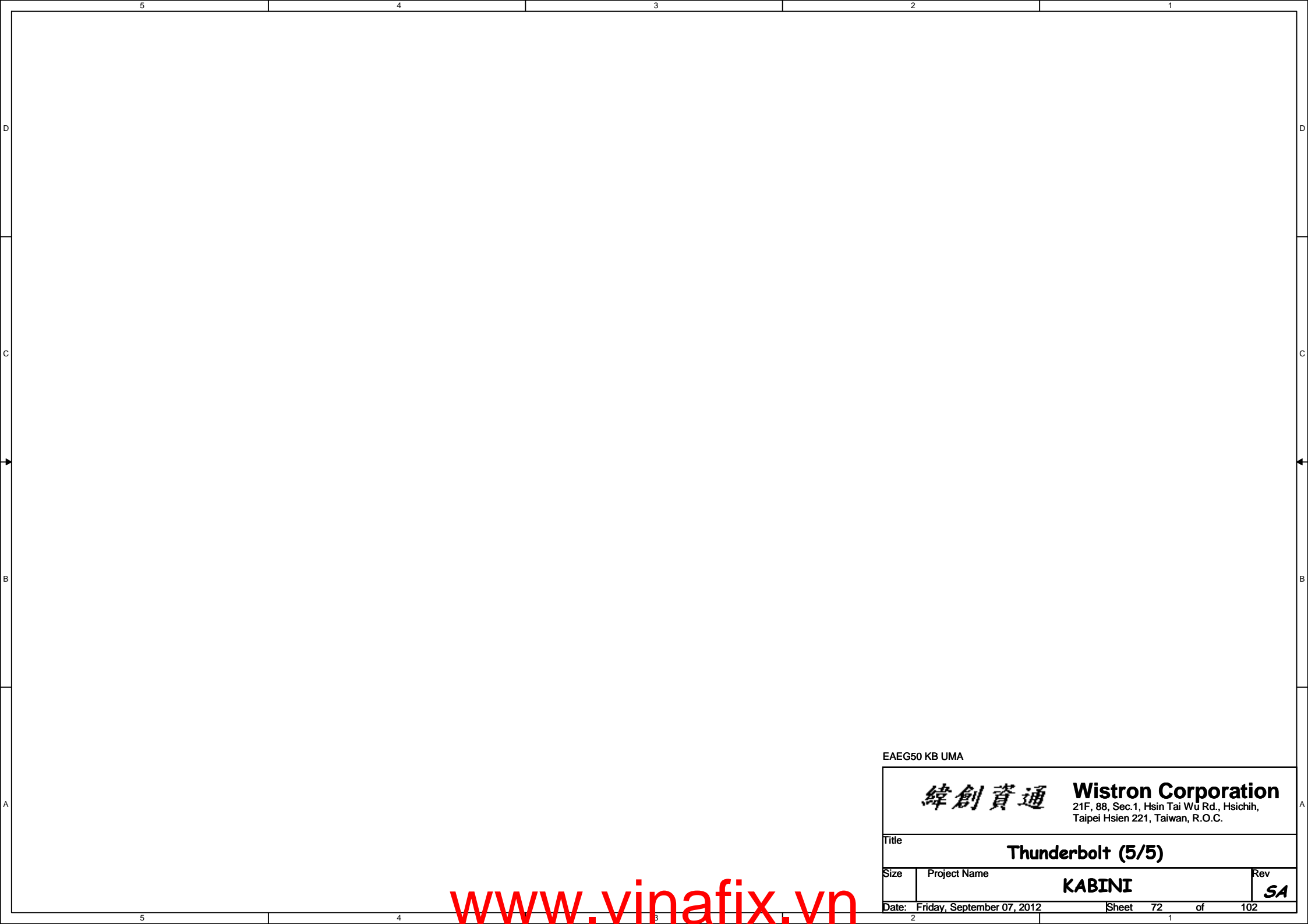
EAEG50 KB UMA

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>Thunderbolt (3/5)</div>		
Size	Project Name <div>KABINI</div>	Rev <div>SA</div>
Date: Friday, September 07, 2012		Sheet 70 of 102




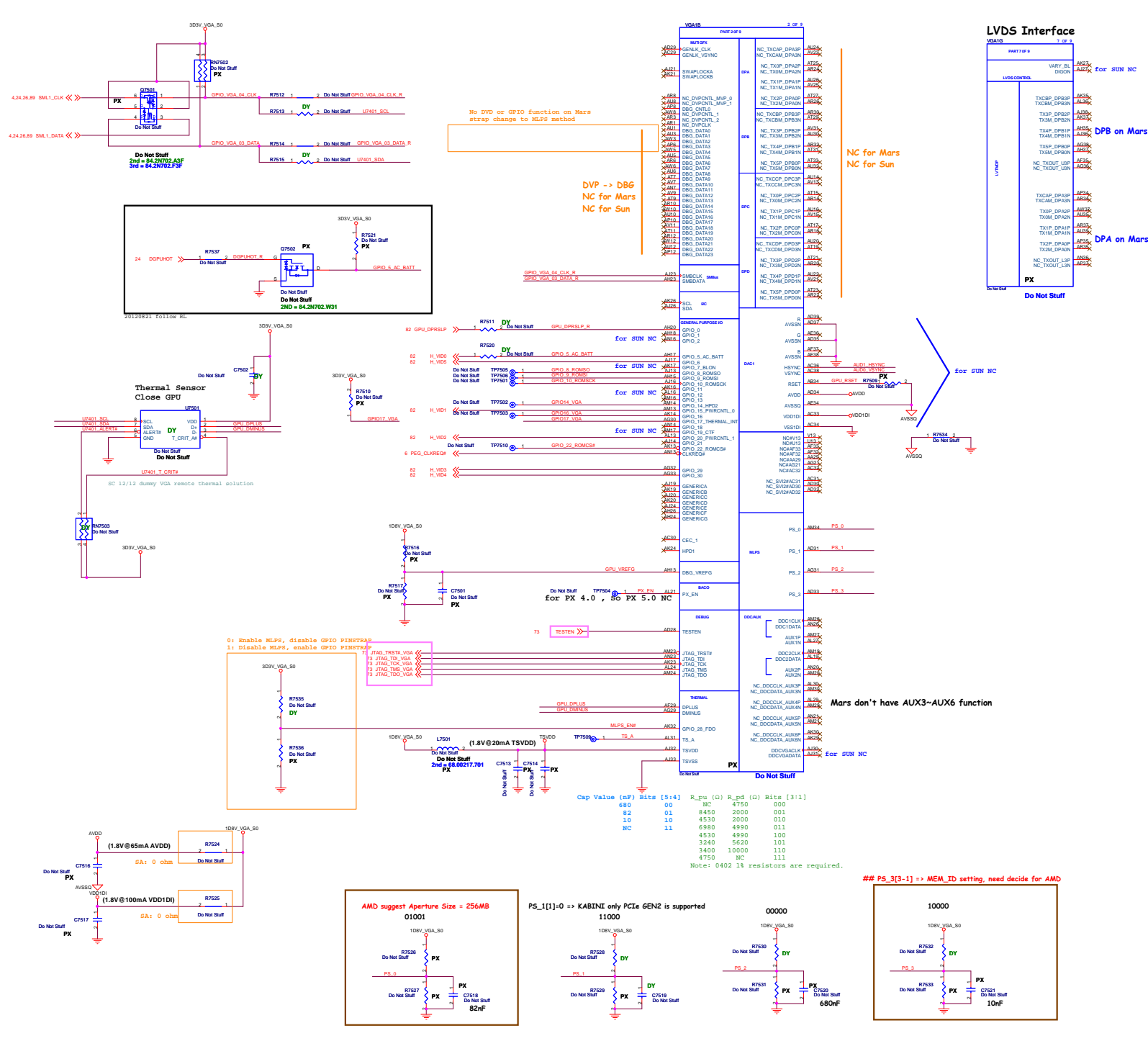
EAEG50 KB UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Thunderbolt (4/5)			
Size	Project Name KABINI		Rev SA
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Title Thunderbolt (5/5)			
Size	Project Name KABINI		Rev SA
Date:	Friday, September 07, 2012	Sheet	72 of 102



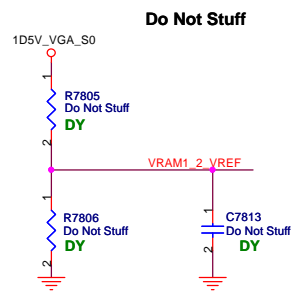
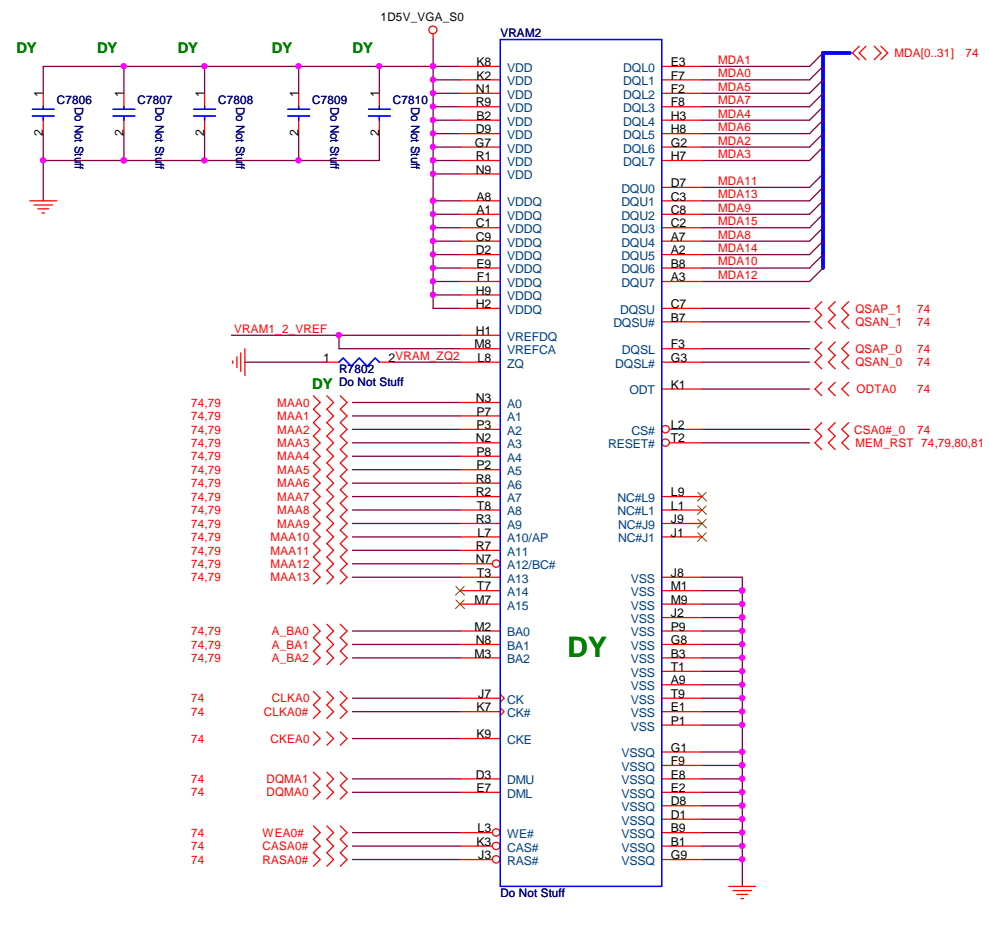
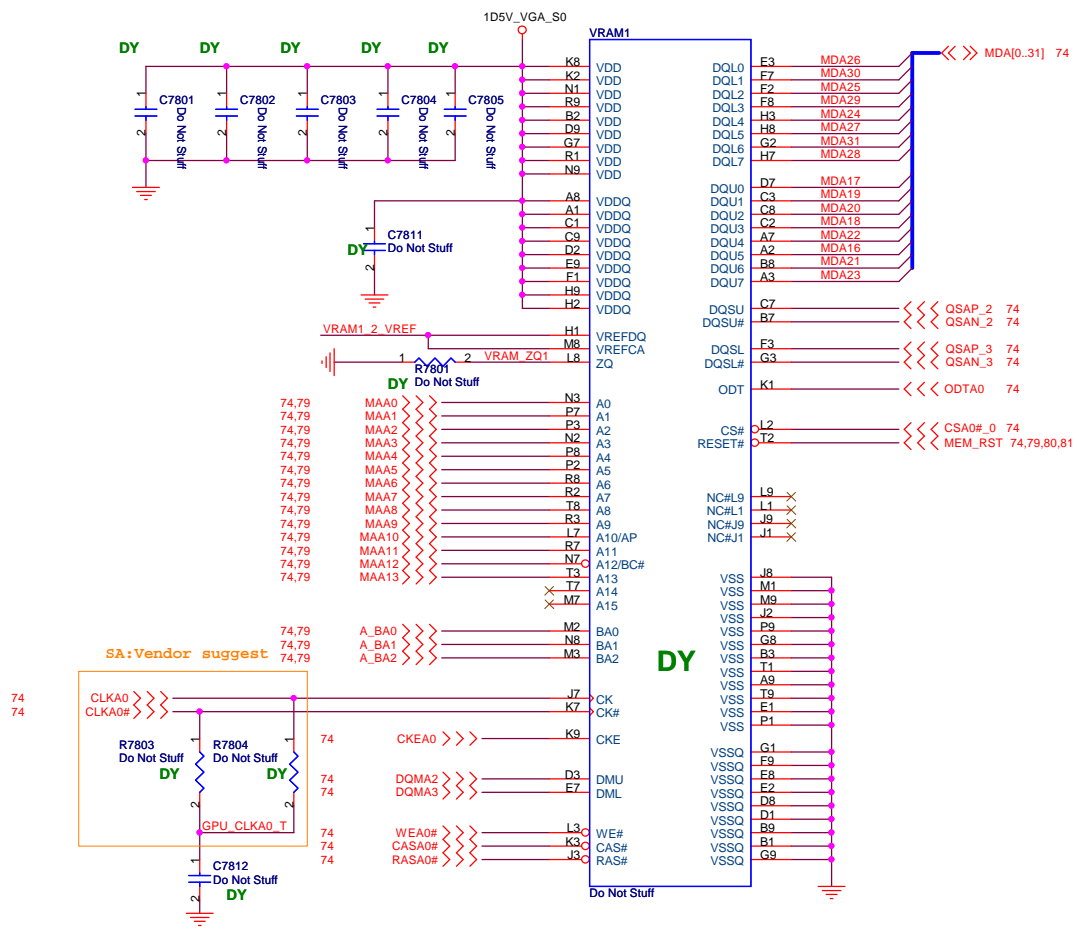
MLPS has setted AUD[1] and AUD[0] but these two strap also need to set

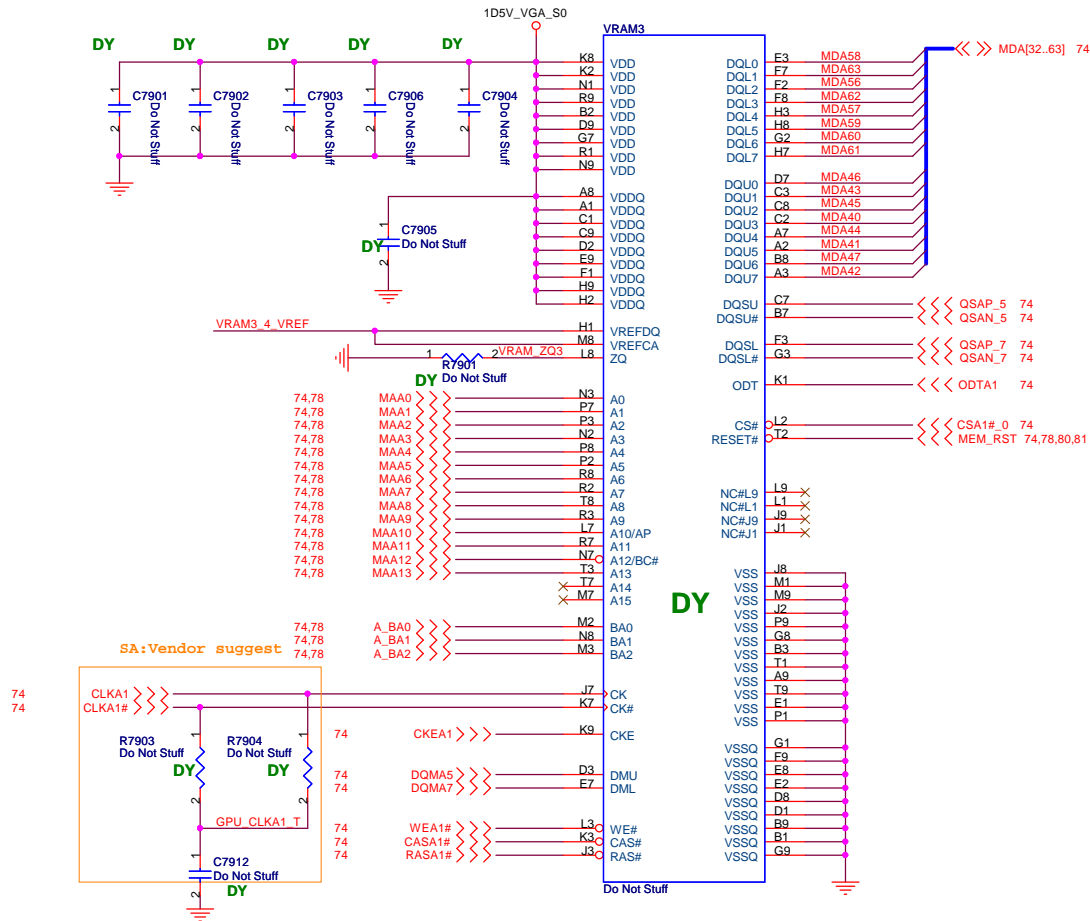
00 = 30 audio function
01 = Audio for DP only
10 = Audio for DP and HDMI if single is detected
11 = Audio for both DP and HDMI
HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

Table 3-11 Multi-Line Pin Straps

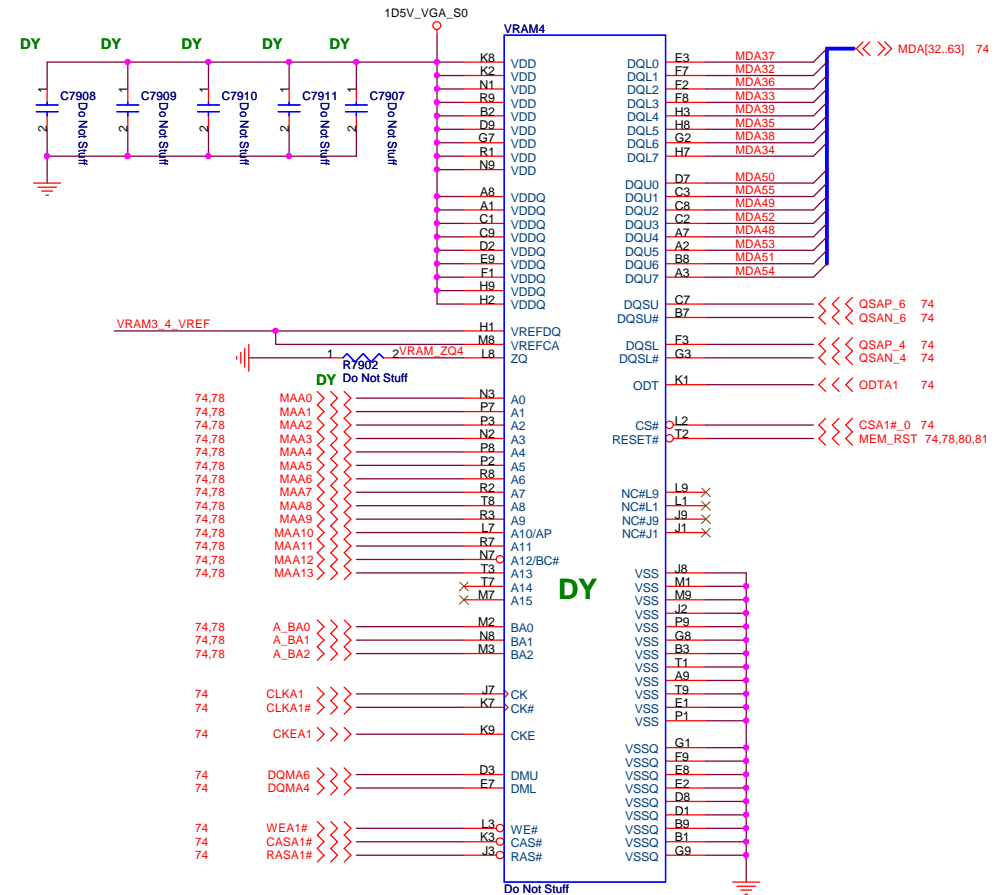
MLPS Bit	Strap Name	Description	Recommended Settings
PS_0[1]	ROM_CONFIG[0]	If STRAP_ROM_ROM_EN = 1, ROM_CONFIG[0] defines the ROM type.	Design dependent, see the description.
PS_0[0]	ROM_CONFIG[1]	If STRAP_ROM_ROM_EN = 0, ROM_CONFIG[1] defines the primary memory aperture size. See Primary Memory Aperture Size (p. 68).	Design dependent, see the description.
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[3]	AUD_PORT_CON[0]	The CPU audio output port of the strap option that indicates the number of audio-capable display outputs.	Design dependent, see the description.
PS_1[11]	STRAP_BIF_GEN2_ENLA	PCIe GEN2 capability. 1 = PCIe GEN2 is supported. 0 = PCIe GEN2 is not supported.	Design dependent, see the description.
PS_1[23]	STRAP_BIF_GEN2_ENLA	Determines whether or not the PCIe reference clock power management capability is supported in the PCIe configuration space (reference to PCIe CLREF#0).	0
PS_1[23]	STRAP_BIF_GEN2_ENLA	1 = The CLREF#0 power management capability is disabled. 0 = The CLREF#0 power management capability is enabled.	1
PS_1[31]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-swinging mode. 0 = The transmitter full-swinging is enabled. 1 = The transmitter full-swinging is disabled.	1
PS_1[13]	STRAP_TX_DEEPENH_EN	PCI EXPRESS 5.0 transmitter, de-emphasis mode. 0 = Tx de-emphasis disabled. 1 = Tx de-emphasis enabled.	Design dependent, see the description.
PS_1[21]	N/A	Reserved.	N/A
PS_1[22]	N/A	Reserved.	N/A
PS_1[23]	STRAP_ROM_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
MLPS Bit	Strap Name	Description	Recommended Settings
PS_1[24]	STRAP_BIF_VGA_DIS	VGA disable. Determines whether or not the card will be recognized as the system's VGA controller. Through the DDC/VGA_DIS field in the C = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_1[25]	N/A	Reserved.	N/A
PS_1[26]	BOARD_CONFIG[0]	Board configuration related wrapping, such as for memory ID.	Design dependent, see the description.
PS_1[27]	BOARD_CONFIG[1]	Board configuration related wrapping, such as for memory ID.	Design dependent, see the description.
PS_1[28]	BOARD_CONFIG[2]	Board configuration related wrapping, such as for memory ID.	Design dependent, see the description.
PS_1[4]	AUD_PORT_CON[0]	Determines the maximum number of digital display audio outputs that will be presented to the OS and user. That should be set to the maximum number of digital display audio outputs that can be enabled simultaneously in the product, which is limited by the ASIC pins (small, the number and type of recovery on the board (DP, HDMI), and the number of audio for each DP connector (the DP-HDMI audio of the video driver). Cleared endpoints should be disabled. This pin strap is intended as an active low binary as follows to ensure zero enable all endpoints. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	Design dependent, see the description.
PS_1[3]	AUD_PORT_CON[1]		
PS_1[3]	AUD_PORT_CON[2]		

Note: AUD[1] (on BSYNC) and AUD[0] (on VSYNC) still need to be properly pin strapped even in a MLPS-based design.

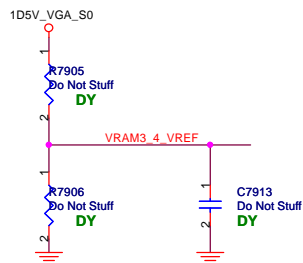




Do Not Stuff



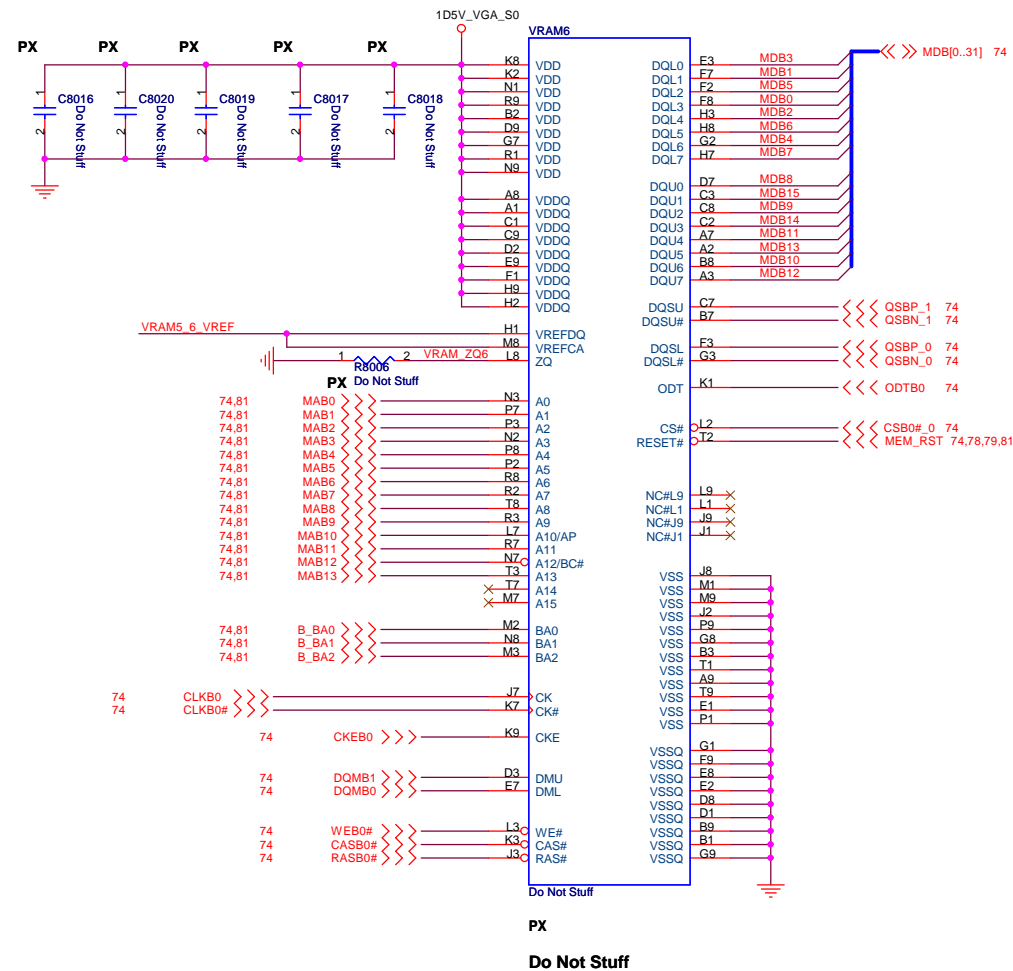
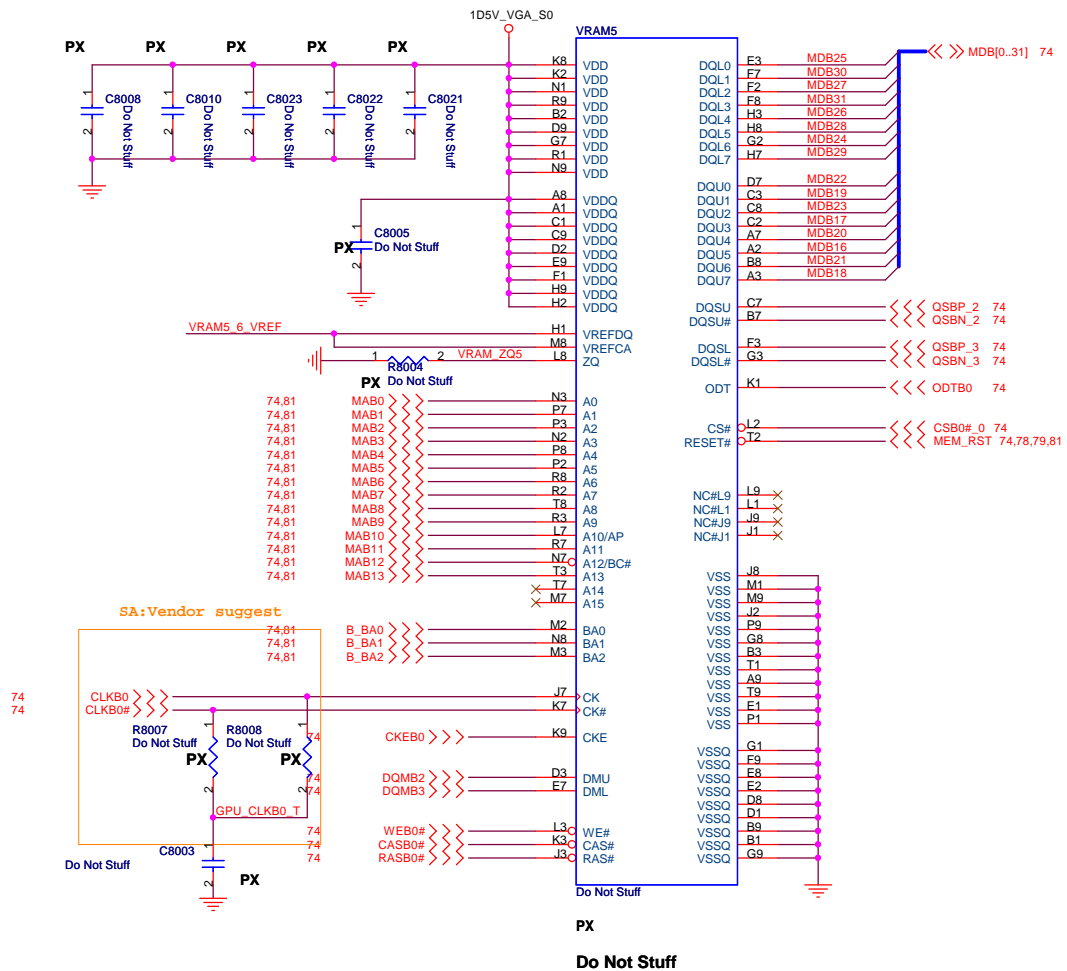
Do Not Stuff



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Title			VRAM 3,4
Size	Project Name	Rev	
		SA	
Date:	Monday, February 04, 2013	Sheet	79 of 102



EG50 VRAM: 72.52G63.C0U (VR.2GB0G.005)
IC VRAM H5TQ2G63DFR-11C FBGA 96P 128M*16 x4

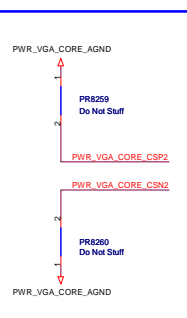
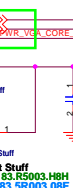
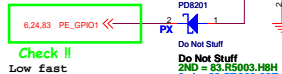
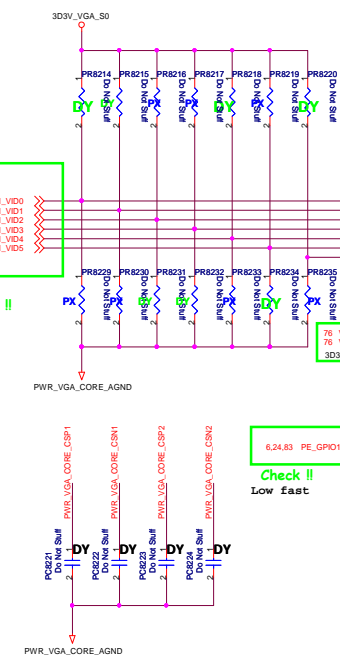
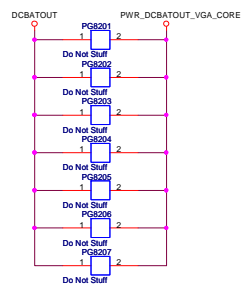
EAEG50 KB UMA

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Taipei Hsien 221, Taiwan, R.O.C.

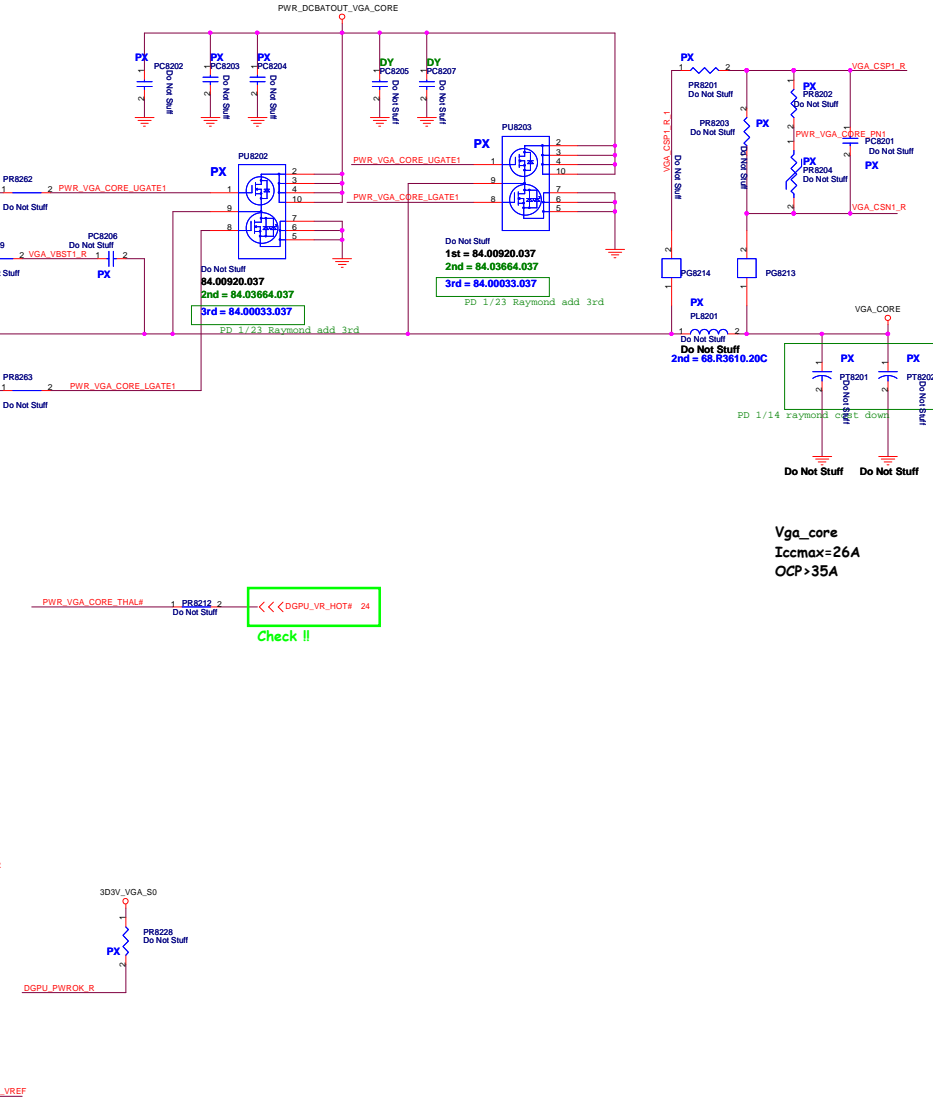
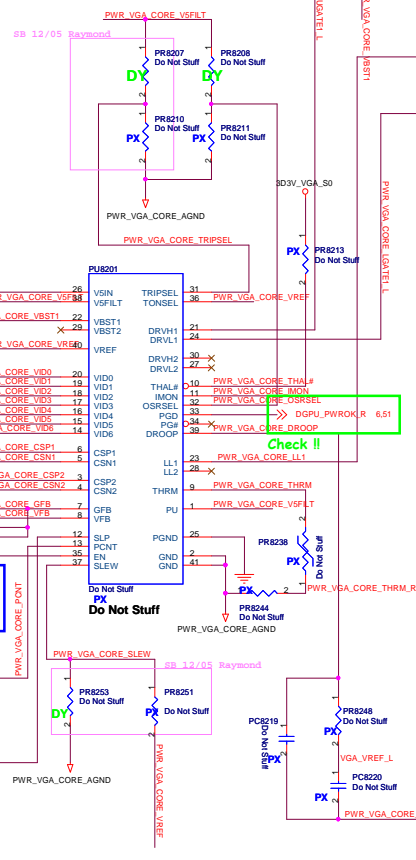
Title			VRAM 5,6
Size	Project Name	KABINI	
Date: Monday, February 04, 2013	Sheet 80	of 102	Rev 5A

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```
SSID = PWR.Plane.Regulator_GFX
```



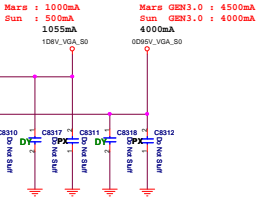
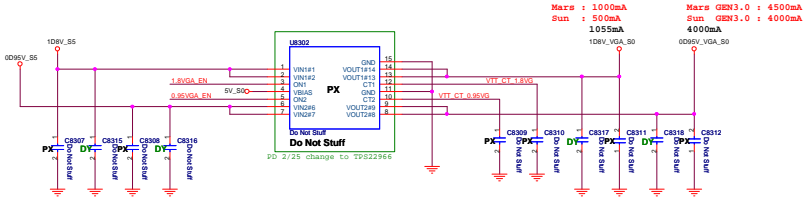
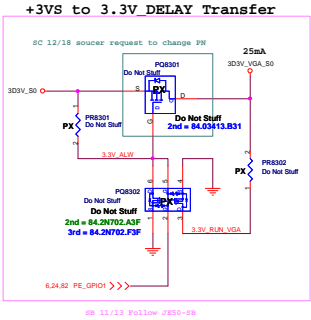
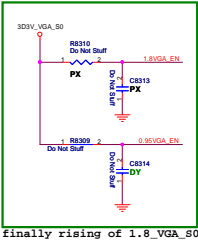
1phase PR8259 , PR8260 mount
2phase PR8259 , PR8260 DY



Vga_core
Iccmax=26A
OCP>35A


APL3523 for VGA_Power

	FE_GP100	FE_GP101
dGPU mode	H	H
IGPU	L	L
IGPU with BACO	H	H





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Title		
Switch GFX		
Size	Project Name	Rev
	KABINI	SA
Date: Friday, September 07, 2012		Sheet 84 of 102

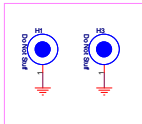


EAEG50 KB UMA

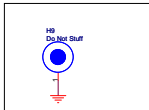
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Switch VGA			
Size	Project Name		Rev
	KABINI		SA
Date: Friday, September 07, 2012		Sheet 85 of 102	

ZZ.00PAD.2N1

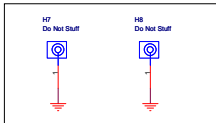
SB 11/14 follow BW for factory issue



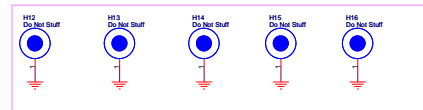
ZZ.00PAD.D01



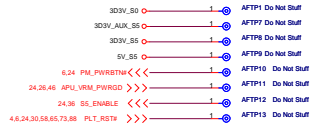
ZZ.00PAD.E01



SB 11/20 ZZ.00pad.2T1 for change BKT size



Check test point



Test Point放在Dimm Door打開可量測處

10/15 follow BW



AD_JK
AD_JK



DC IN connector



Battery connector



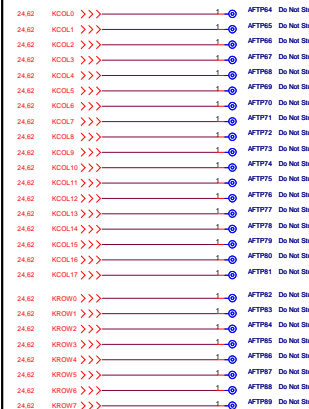
Speaker connector



HP connector



FAN connector



Normal KB connector



Touch Pad connector

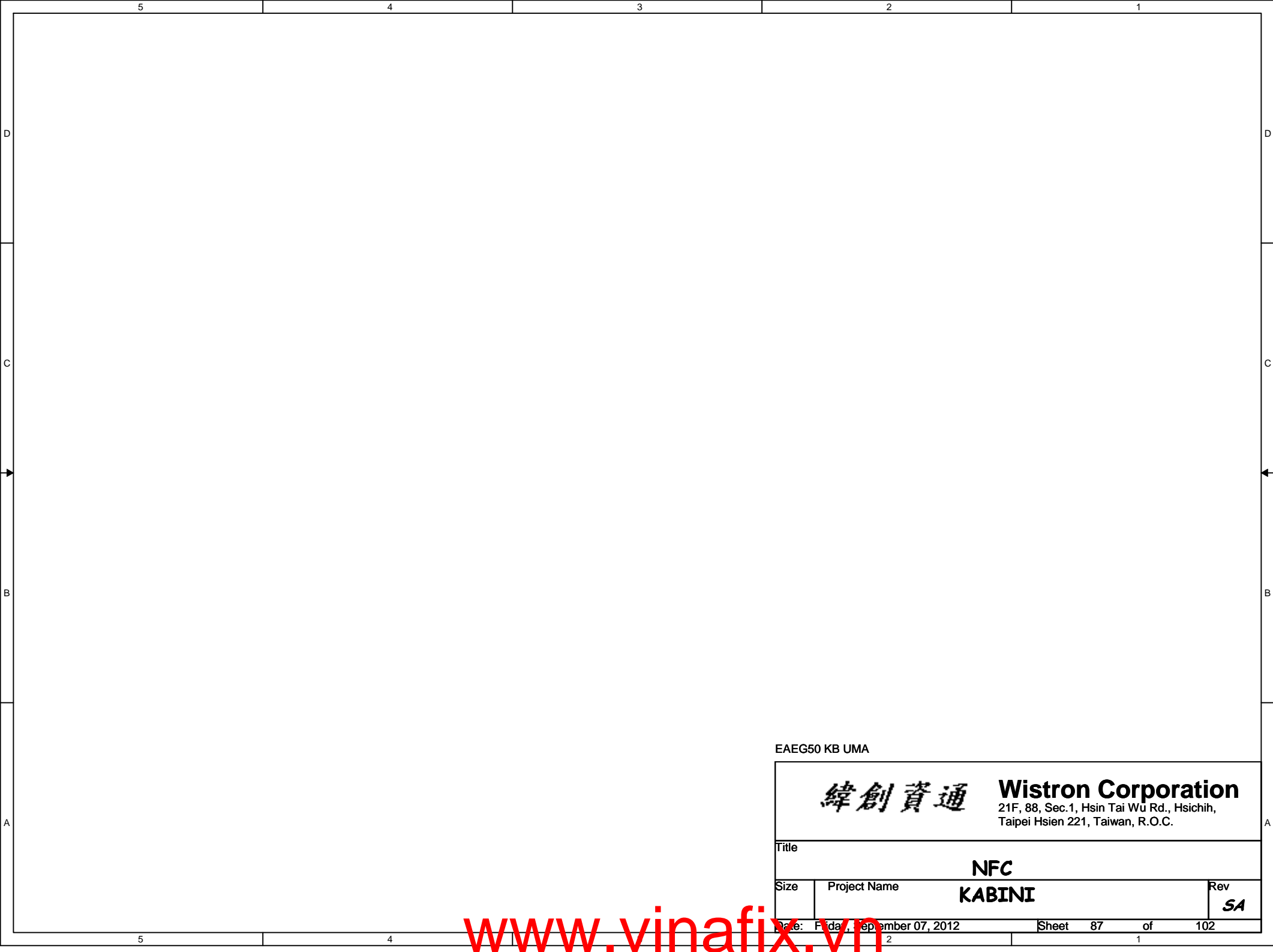


EAE090 KB UAA

緯創資通 Wistron Corporation
21F, 8th, Sec. 1, Hsin-Tai Rd, Hsinchu, Taiwan 301, Taiwan, R.O.C.

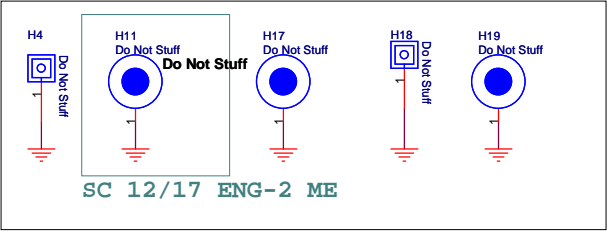
UNUSED PARTS/FMT Capacitors				
Item	Project	CA	NT	
1	Monday, Feb 20, 2018	Result	85	100

www.vinafix.vn

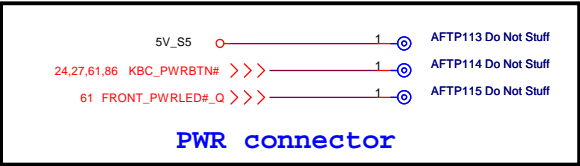


www.vinafix.vn

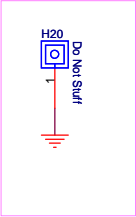
H4 & H11 & H17 & H18 & H19 for EG50



PWRBD AFTP for EG50

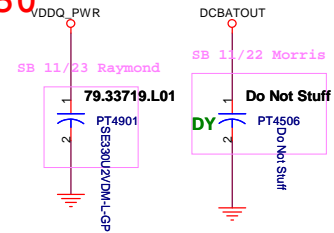
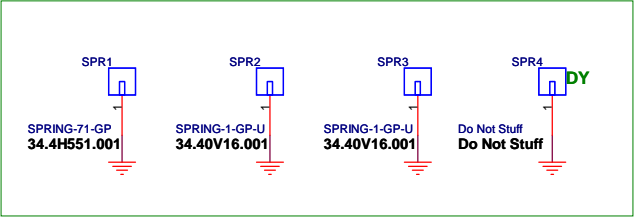


ZZ.00PAD.571



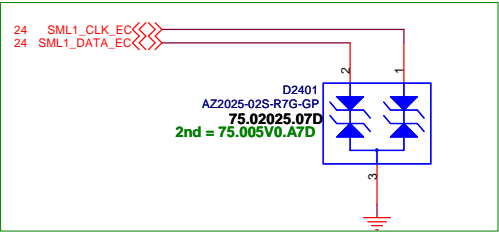
SB 11/20 location same with 14" H2

PD 1/23 EMI Jen



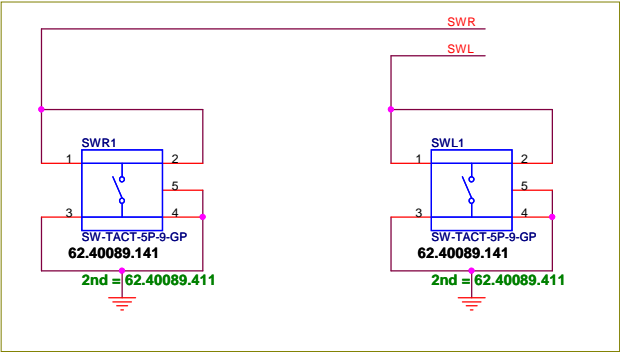
SB 11/23 3mm high limit in EG50

PD 01/31 Different Net name in 14" & 15" for placement



24,62,86	KCOL0	>>>
24,62,86	KCOL1	>>>
24,62,86	KCOL2	>>>
24,62,86	KCOL3	>>>
24,62,86	KCOL4	>>>
24,62,86	KCOL5	>>>
24,62,86	KCOL6	>>>
24,62,86	KCOL7	>>>
24,62,86	KCOL8	>>>
24,62,86	KCOL9	>>>
24,62,86	KCOL10	>>>
24,62,86	KCOL11	>>>
24,62,86	KCOL12	>>>
24,62,86	KCOL13	>>>
24,62,86	KCOL14	>>>
24,62,86	KCOL15	>>>
24,62,86	KCOL16	>>>
24,62,86	KCOL17	>>>
24,62,86	KROW0	>>>
24,62,86	KROW1	>>>
24,62,86	KROW2	>>>
24,62,86	KROW3	>>>
24,62,86	KROW4	>>>
24,62,86	KROW5	>>>
24,62,86	KROW6	>>>
24,62,86	KROW7	>>>

For AFTE



PD 1/21
SWL1 / SWR1 1st change to 62.40089.141, 2nd change to 62.40089.411 ,
because 160kg change to 100kg.

EAEG50 KB UMA

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
15"			
Size	Project Name		Rev
	KABINI		5A
Date:	Monday, February 25, 2013	Sheet	90 of 102



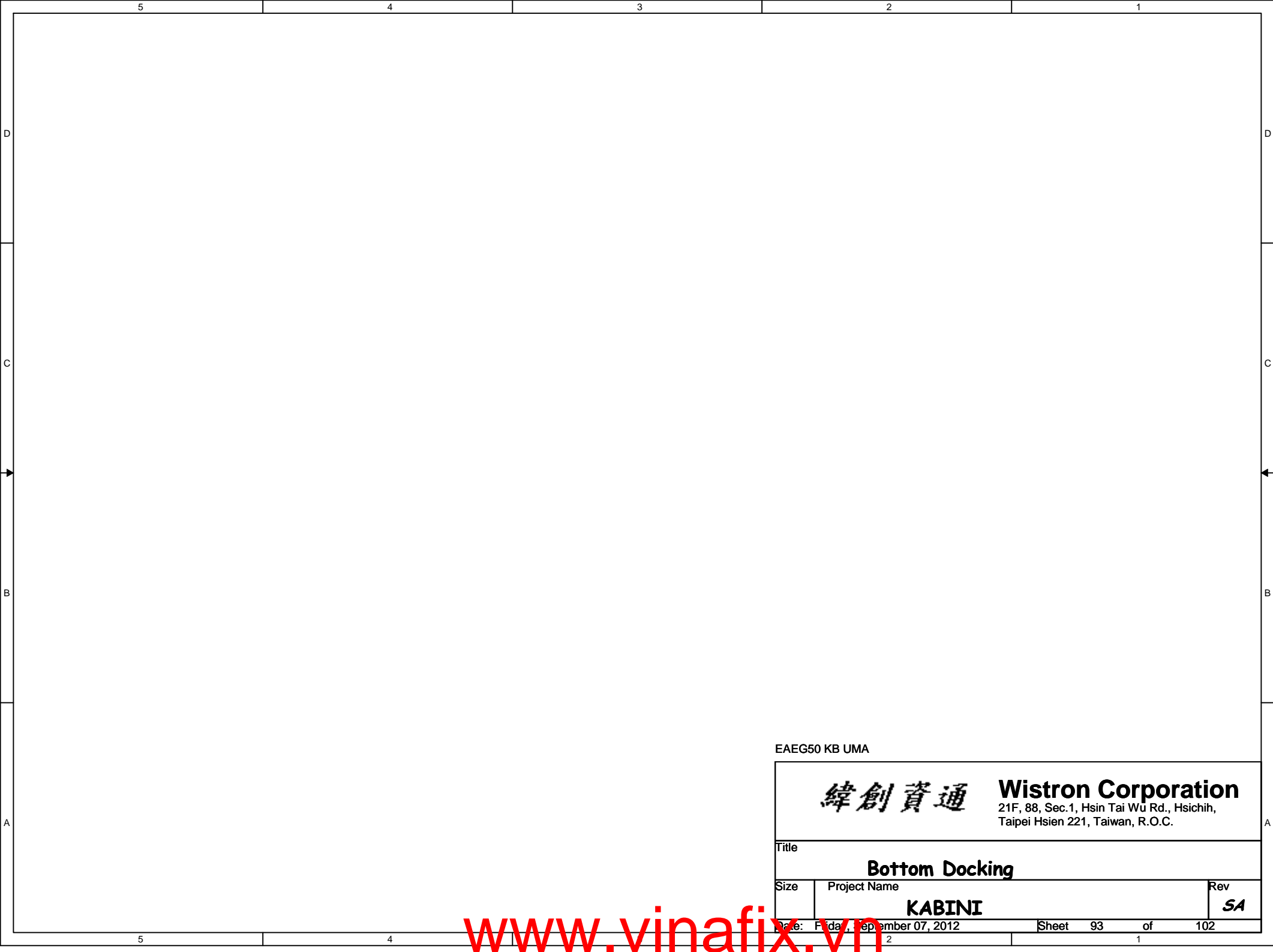
EAEG50 KB UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Smart Card socket			
Size	Project Name		Rev
	KABINI		SA
Date: Friday, September 07, 2012		Sheet	91 of 102



EAEG50 KB UMA

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>	
Title	
Switchable GFX eDP	
Size	Rev
Project Name	
KABINI	
SA	
Date: Friday, September 07, 2012	Sheet 92 of 102



EAEG50 KB UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Bottom Docking			
Size	Project Name		Rev
	KABINI		SA
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EAEG50 KB UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Inter LAN WG1217LM		
Size	Project Name	Rev
	KABINI	SA
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EAEG50 KB UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LAN Switch			
Size	Project Name		Rev
	KABINI		SA
Date: Friday, September 07, 2012		Sheet	95 of 102



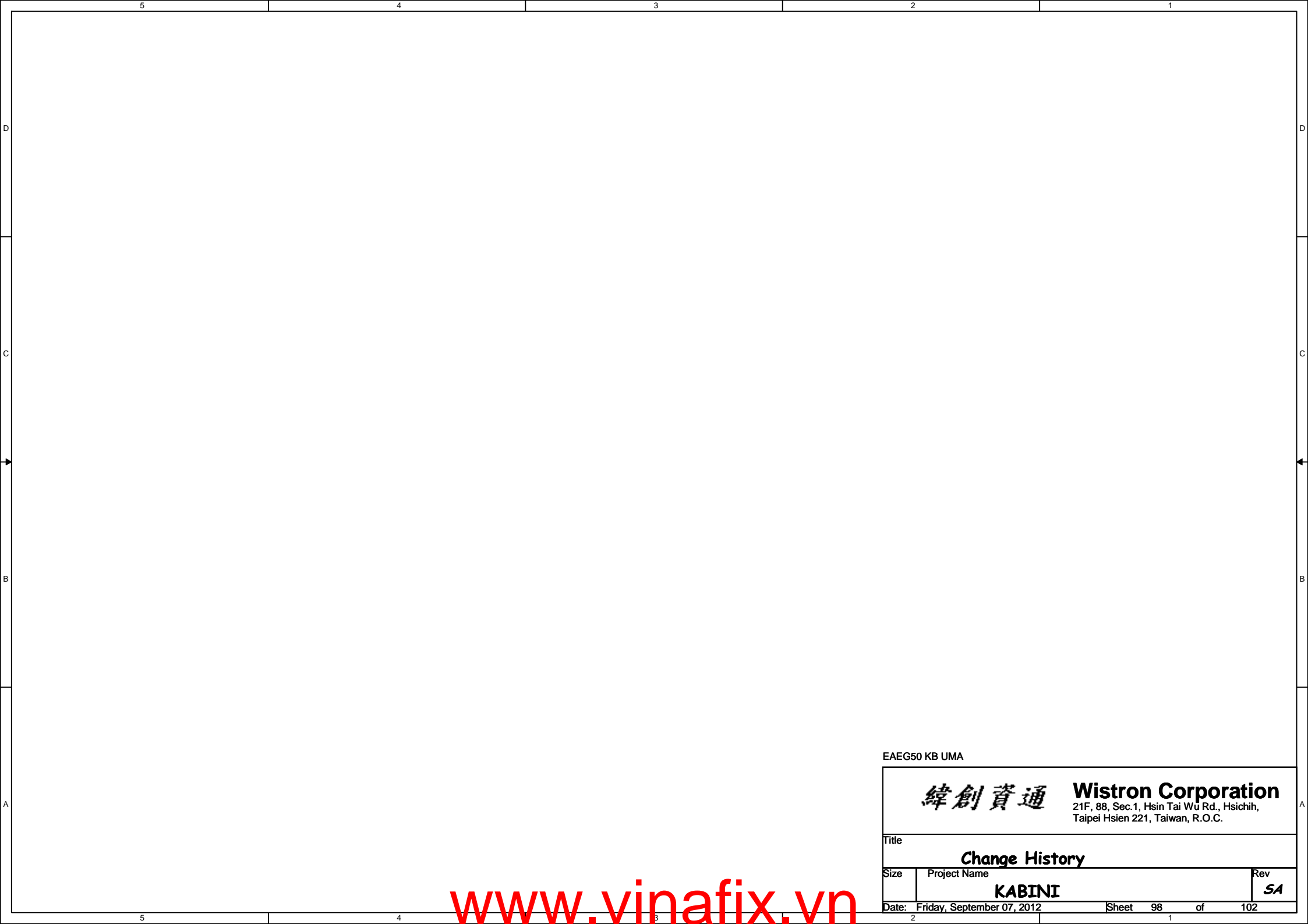
EAEG50 KB UMA

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title PCH_XDP	
Size	Project Name KABINI
Date: Friday, September 07, 2012	Rev SA
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EAEG50 KB UMA

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>	
Title	
table of content	
Size	Rev
Project Name	
KABINI	
SA	
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5

4

3

2

1

D

D

C

C

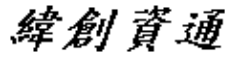
B

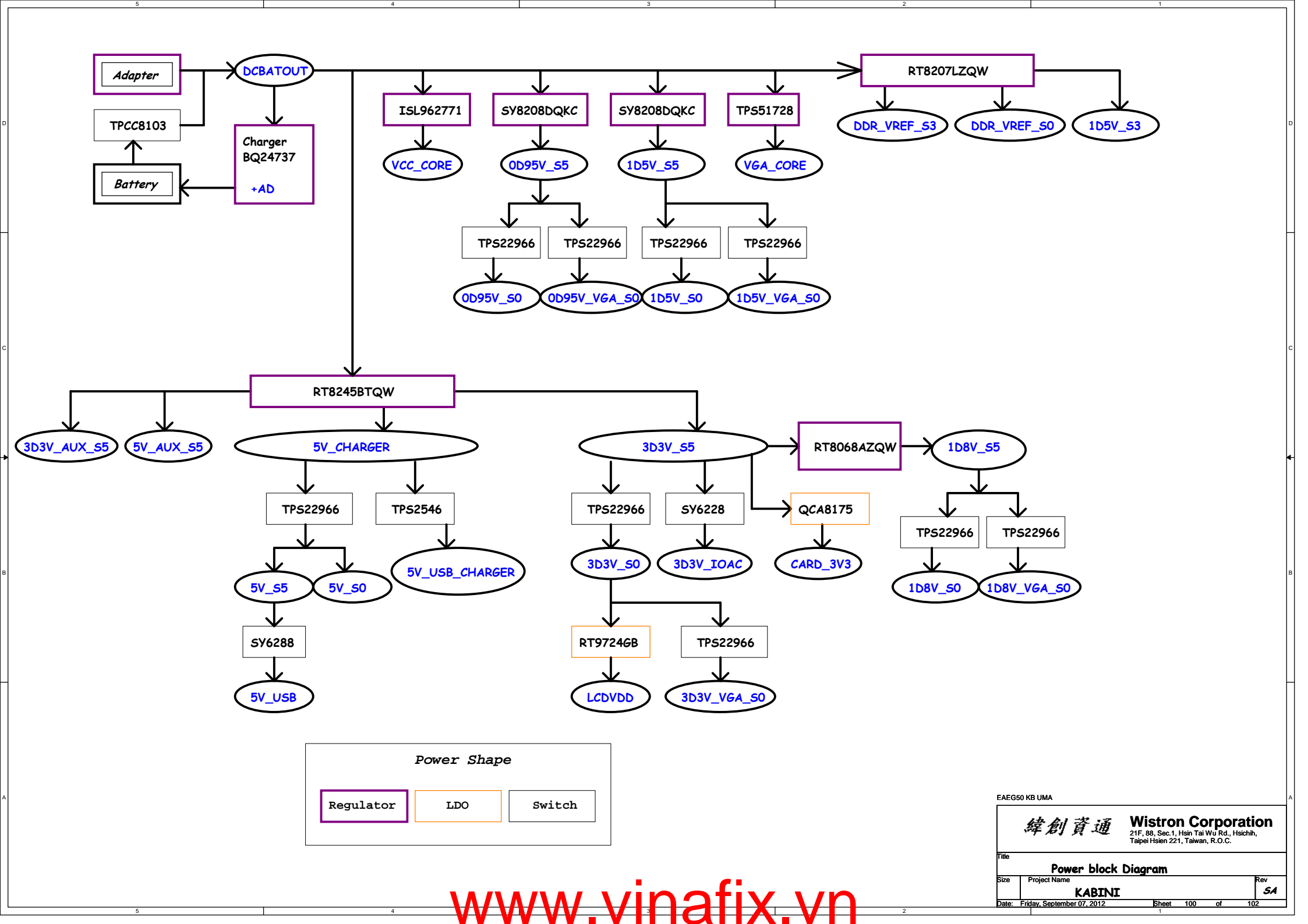
B

A

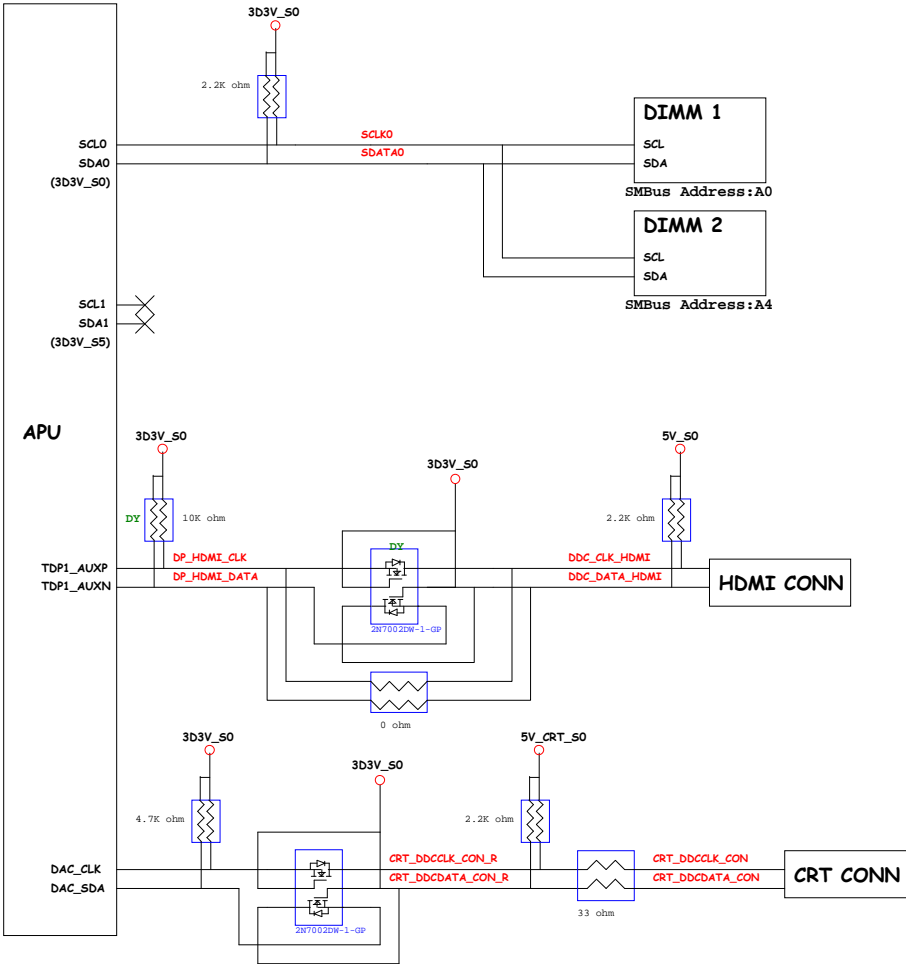
A

EAEG50 KB UMA

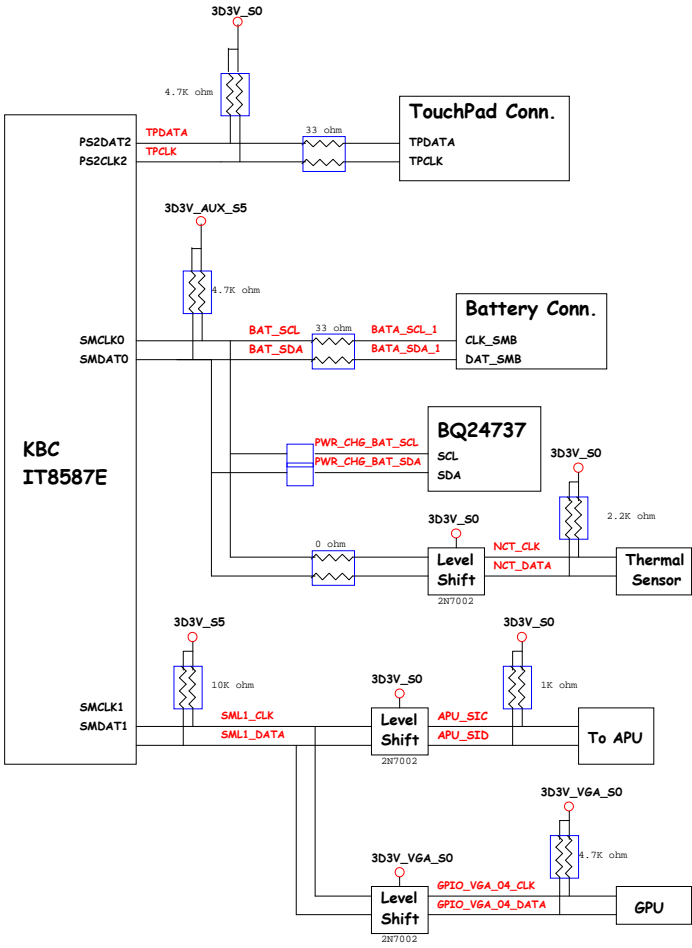
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Change History			
Size	Project Name		Rev
	KABINI		SA
Date:	Friday, September 07, 2012	Sheet	98 of 102



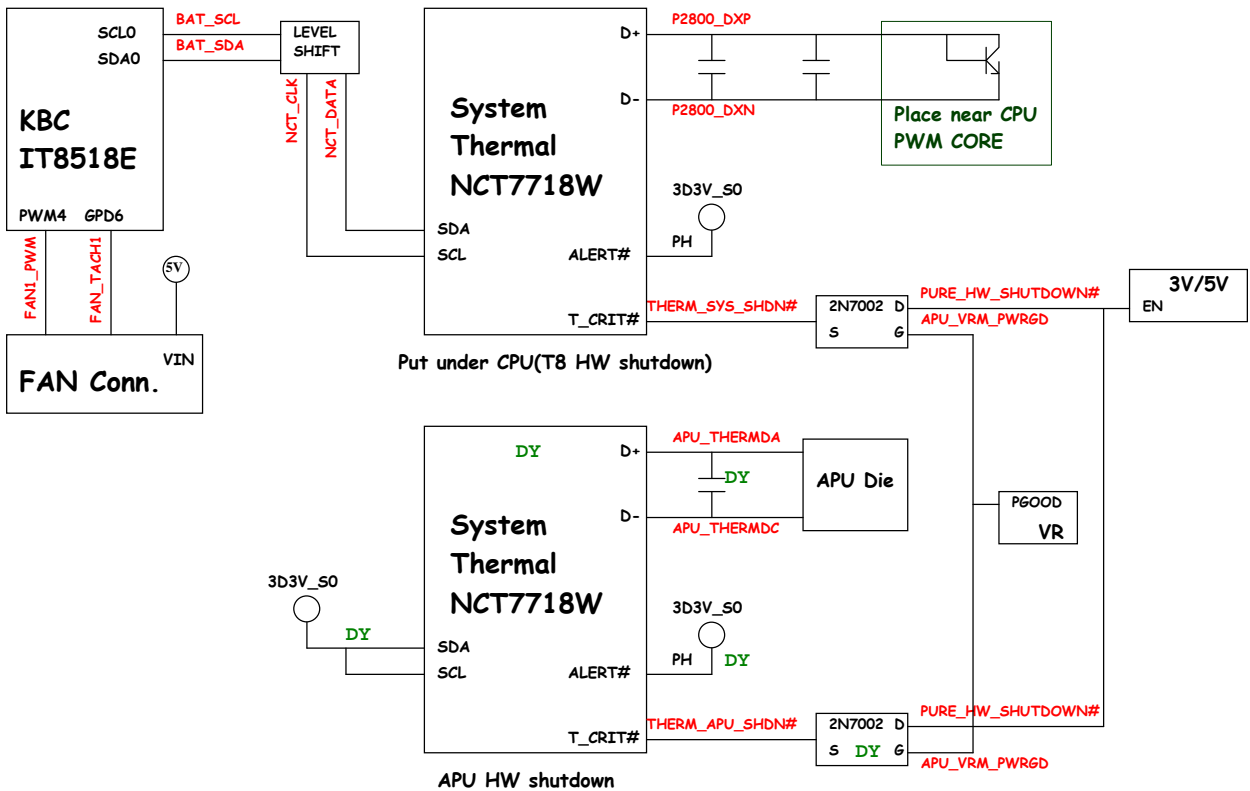
SMBus Block Diagram



KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram

